

UTE

Spécification française harmonisée
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CECC 90 101-051

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Nombre total de pages : 19

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**COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :**

**ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :**

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 71

Adoptée le 16 novembre 1987

BS9440 F718 to F730

Issue 1

June, 1978

DESSIN ET DIMENSIONS :

OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 09 - 050 G 08
IEC 191-2 -

Référence française : F 117 - F 117A
French reference :

**IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS**

Voir Tableau II
See Table II

**SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRA-
TED CIRCUITS IN ACCORDANCE WITH FS 90 101**

54/64/74 173

**REGISTRE DE 4 ELEMENTS BINAIRES
SORTIES 3 ETATS DE PUISSANCE**

**4-BIT D-TYPE REGISTER
WITH 3-STATE OUTPUTS**

**TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :**

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.

**NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :**

AMENDMENTS TO THE FOLLOWING CLAUSES

§ 2 - Add :

Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$

§ 3 To be replaced by CECC 90 000/3 § 2.5

§ 4 To be deleted

§ 5 To be replaced by CECC 90 000/3 § 2.6

§ 6 To be replaced by CECC 90 000/3 § 4.10.1

§ 7 All inspection level and AQL are those specified in 90 100/3.

Replace A3b by A4a, A3c by A4b, A4 by A5.

Add A8 of 90 100/3 (Assessment level P only).

Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.

For groups B, C, D, apply 90 100/3.

Sub-groups A6, A7 : not applicable.

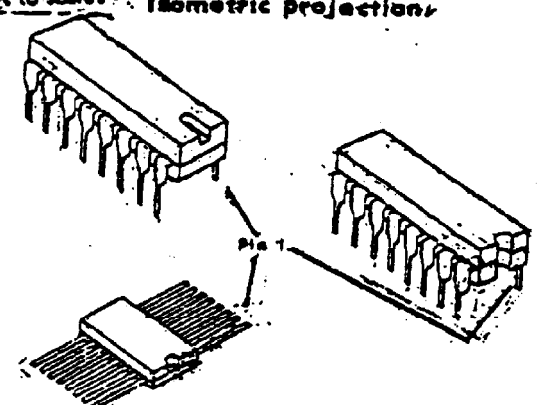
Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.



Documents

Document Sharing Hub

BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON, W1A 2BS	BS 9440 F718 to F730 ISSUE 1 JUNE, 1978
Specification available from:— As shown in PD 9002 and :	Page 1 of 18 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH BS 9440 Issue 2	MANUFACTURER'S TYPE NUMBER 54173 64173 74173
Outlines not to scale. Isometric projections.  For details dimensions: — 16-lead Flat Pack — see Appendix 1 16-lead Dual in-line — see BS 3934 SO-8IC Marking information: — Clause 3	See PD 9002 For ordering information: — see Clause 5. SILICON MONOLITHIC TTL 4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUT CERAMIC/GLASS HERMETICALLY SEALED ENCAPSULATION OR DUAL-IN-LINE PLASTIC ENCAPSULATION FULL ASSESSMENT LEVEL AND APPLICATION CATEGORIES S1, S2, S3 and S4

1.	Limiting Conditions of Use (not for inspection purposes)	
	Absolute values (non-simultaneous)	
V_{CC}	Maximum continuous positive supply voltage	7.0 V
	Maximum continuous negative supply voltage	0.5 V
	Maximum continuous positive input voltage	7.0 V
	Maximum continuous negative input voltage (non-clamping mode)	0.5 V
	Maximum negative input current (clamping mode)	18.0 mA
	Maximum reverse input current	0.1 mA
T_{amb}	Ambient operating temperature range	-55 to +125 °C
		-40 to +85 °C
		0 to +70 °C
T_{stg}	Storage temperature range	-65 to +150 °C
	Shock (0.5 ms duration)	14 700 m/s ²
	Vibration	196 m/s ²

Refer to Qualified Products List PD 9002 for details of manufacturers approved to this specification.

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2. Recommended Conditions of Use and Associated Characteristics
(not for inspection purposes)

These characteristics apply over the ambient operating temperature range unless otherwise stated.

		Min.	Max.	Unit
V_{CC}	Positive supply voltage	4.5	5.5	V
	54173 64173 & 74173	4.75	5.25	V
V_{IH}	HIGH state input voltage	2.0	5.5	V
I_{CC}	Total supply current per package at V_{CC} maximum value	-	72.0	mA
V_{OH}	HIGH state output voltage	2.4	-	V
V_{IL}	LOW state input voltage	0	0.8	V
V_{OL}	LOW state output voltage	-	0.4	V
$-V_{IC}$	Input clamping voltage at $-I_{IN} = 12.0$ mA	-	1.5	V
$I_{IH(1)}$	HIGH state input current $V_{IN} = 5.5$ V	-	1.0	mA
$I_{IH(2)}$	HIGH state input current $V_{IN} = V_{OH}$ minimum	-	40.0	μ A
$-I_{IL}$	LOW state input current $V_{IN} = V_{OL}$ maximum	-	1.6	mA
I_{OL}	LOW state output current	-	16.0	mA
$-I_{OH}$	HIGH state output current	-	2.0	mA
	54173 64173 & 74173	-	5.2	mA
$-I_{OS}$	Output short circuit current	30.0	70.0	mA
I_O	High impedance (off state) output current $V_{OUT} = 2.4$ V	-	40.0	μ A
	$V_{OUT} = 0.4$ V	-	-40.0	μ A

Switching Characteristics

$V_{CC} = 5.0$ V, $T_{amb} = 25$ °C, $C_L = 50$ pF, $R_L = 400$ Ω

t_{PHL}	Clock input to output	-	31.0	ns
	Clear input to output	-	27.0	ns
t_{PLH}	Clock input to output	-	43.0	ns
t_{PZH}	Output enable to HIGH level	-	30.0	ns
t_{PZL}	Output enable to LOW level	-	30.0	ns
	$C_L = 5.0$ pF			
t_{PHZ}	Output disable from HIGH level	-	14.0	ns
t_{PLZ}	Output disable from LOW level	-	20.0	ns

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2. Recommended Conditions of Use and Associated Characteristics (Contd..)

		Min.	Max.	Unit.
$f_{\max}$	Maximum clock frequency	25.0	0	MHz
$t_{p(\text{clear or clock})}$	Duration of clear or clock pulse	20.0	-	ns
$t_{p(\text{set-up Data enable})}$	Duration of Data enable pulse	17.0	-	ns
$t_{p(\text{set-up data})}$	Duration of data pulse	10.0	-	ns
$t_{p(\text{enable})}$	Duration of M or N to clear disable state	10.0	-	ns
$t_{(\text{hold data})}$	Data hold time	10.0	-	ns
$t_{(\text{hold enable})}$	Data enable hold time	2.0	-	ns



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Table I

Function Table.

INPUTS					OUTPUT Q
CLEAR	CLOCK	DATA ENABLE G1 G2		DATA D	
H	X	X	X	X	L
L	L	X	X	X	Q ₀
L	↑	H	X	X	Q ₀
L	↑	X	H	X	Q ₀
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high impedance state; however, sequential operation of the flip-flops is not affected.

H = HIGH state

L = LOW state

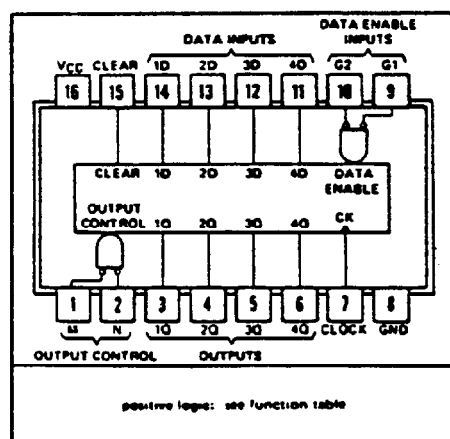
↑ = Transition from LOW to HIGH level

Q₀ = level of Q_c before the indicated conditions were established.

X = OFF (High Impedance) state of a 3-state output

Table II

Logic Diagram and Connections



3. MARKING.

3.1 Each integrated circuit shall bear the following markings:

- (a) Terminal identification.
- (b) The manufacturer's type number.
- (c) The factory identification code, or manufacturer's trade mark.
- (d) The date code.

3.2 Each package containing one or more of these circuits shall bear the markings (b), (c) and (d) above and in addition:

- (e) The B.S. detail specification number.

4. RELATED DOCUMENTS.

- BS 2011 Basic environmental testing procedures.
- BS 3934 Dimensions of semiconductor devices.
- BS 6001 Sampling procedures and tables for inspection by attributes.
- BS 9000 General requirements for electronic components of assessed quality.
- BS 9400 Integrated electronic circuits of assessed quality: Generic data and methods of test.
- PD 9002 Qualified Products List for electronic components of assessed quality.

5. ORDERING INFORMATION.

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification
 as detailed in PD 9002 to BS9440 F..... as defined below -

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual-in-line and Flatpack	54173	F718	F719	F720	F721	F722
	64173	.	F723	F724	F725	F726
	74173	.	F727	F728	F729	F730
PLASTIC Dual-in-line	54173	.	.	.	.	F722
	64173	.	.	.	.	F726
	74173	.	.	.	.	F730

Note: . Not available at present.