

UTE

Spécification française harmonisée
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CECC 90 101-053

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 Nombre total de pages : 14
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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
*ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :*

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 73

Adoptée le 16 novembre 1987

BS9420 F055 to F057

BS9420 F073 to F075

BS9420 F161 to F167

Issue 1

April, 1978

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 09 - 050 G 08
IEC 191-2 -

Référence française : F 117 - F 117A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
*DETAIL SPECIFICATION FOR DIGITAL INTEGRATED
CIRCUITS IN ACCORDANCE WITH FS 90 101*

54/64/74 175

BASCULE BISTABLE TYPE D
QUAD D-TYPE BISTABLE

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

*Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.*

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :

AMENDMENTS TO THE FOLLOWING CLAUSES

§ 2 - Add :

Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$

- Page 2, t_{PHL} "Low state to high state" parameter : replace t_{PHL} by t_{PLH}

§ 3 To be replaced by CECC 90 000/3 § 2.5

§ 4 To be deleted

§ 5 To be replaced by CECC 90 000/3 § 2.6

§ 6 To be replaced by CECC 90 000/3 § 4.10.1

§ 7 All inspection level and AQL are those specified in 90 100/3.

Replace A3b by A4a, A3c by A4b, A4 by A5.

Add A8 of 90 100/3 (Assessment level P only).

Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.

For groups B, C, D, apply 90 100/3.

Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

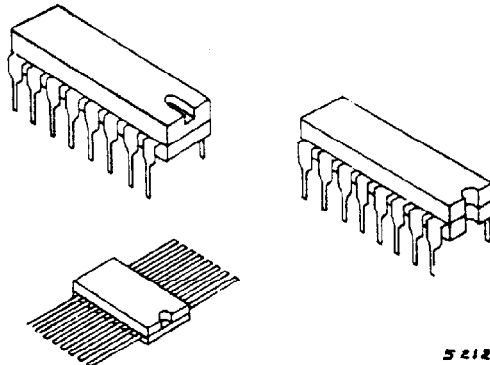
BRITISH STANDARDS INSTITUTION
2 PARK STREET,
LONDON W1A 2BS

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ELECTRONIC COMPONENTS OF ASSESSED QUALITY: DETAIL SPECIFICATION

Outlines not to scale



For detail dimensions:
16 Lead Flat-Pack – see Appendix I
16 Lead Dual in-line – see BS 3934 SO-87C

SILICON MONOLITHIC TTL
QUADRUPLÉ D-TYPE BISTABLE

FULL ASSESSMENT LEVEL
AND APPLICATION CATEGORIES
S1, S2, S3 and S4

TYPES:

54175
64175
74175

See clause 5

CERAMIC/GLASS HERMETICALLY
SEALED ENCAPSULATION OR
DUAL IN-LINE PLASTIC
ENCAPSULATION

1. Limiting conditions of use (not for inspection purposes)

Absolute values (non-simultaneous)

			Units
V_{CC}	Maximum continuous positive supply voltage	7.0	V
	Maximum continuous negative supply voltage	0.5	V
	Maximum continuous positive input voltage	5.5	V
	Maximum continuous negative input voltage	0.5	V
$-I_{IL}$	Maximum input current	1.6	mA
	Maximum reverse input current	1.0	mA
T_{amb}	Ambient operating temperature range	54175 –55 to +125	°C
		64175 –40 to +85	°C
		74175 0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C
	Shock (0.5 ms duration)	14 700	m/s ²
	Vibration	196	m/s ²

Copies of this specification are available from manufacturers listed in the Qualified Products List, Part 1 of PD 9002.

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2. Recommended conditions of use and associated characteristics (not for inspection purposes)

Over the full ambient operating temperature range unless otherwise stated.

			Min.	Max.	Units
V_{CC}	Positive supply voltage	54175	4.5	5.5	V
		64175 & 74175	4.75	5.25	V
I_{CC}	Total supply current per package			45.0	mA
V_{IH}	HIGH state input voltage	54175	2.0	5.5	V
		64175 & 74175	2.0	5.25	V
V_{IL}	LOW state input voltage		0	0.8	V
V_{OH}	HIGH state output voltage		2.4		V
V_{OL}	LOW state output voltage			0.4	V
$I_{IH(1)}$	HIGH state input current, $V_{IN} = V_{IH}$ maximum value			1.0	mA
$I_{IH(2)}$	HIGH state input current, $V_{IN} = 2.4V$			40.0	μA
$-I_{IL}$	LOW state input current, $V_{IL} = 0.4V$			1.6	mA
$-I_{OH}$	HIGH state output current			800.0	μA
I_{OL}	LOW state output current			16.0	mA
$-I_{OS}$	Output short-circuit current	54175	20.0	57.0	mA
		64175 & 74175	18.0	57.0	mA
t_{PHL}	HIGH state to LOW state propagation time at 25°C*				
		From Clock input		30.0	ns
		From Clear input		35.0	ns
t_{PLH}	LOW state to HIGH state propagation time at 25°C*				
		From Clock input		30.0	ns
		From Clear input		25.0	ns
$t_{p(clock)}$	Duration of Clock pulse		20.0		ns
$t_{p(clear)}$	Duration of Clear pulse		20.0		ns
t_{set-up}	Minimum set-up time		20.0		ns
$f_{(clock)}$	Clock frequency			>25.0	MHz
$t_{(hold)}$	Minimum hold time		5.0		ns

*See subgroup A4 for details.

Table 1

Function table (per bistable)

Inputs			Outputs	
Clear	Clock	D	Q	$\bar{Q}$
L	X	X	L	H
H	$\uparrow$	H	H	L
H	$\uparrow$	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

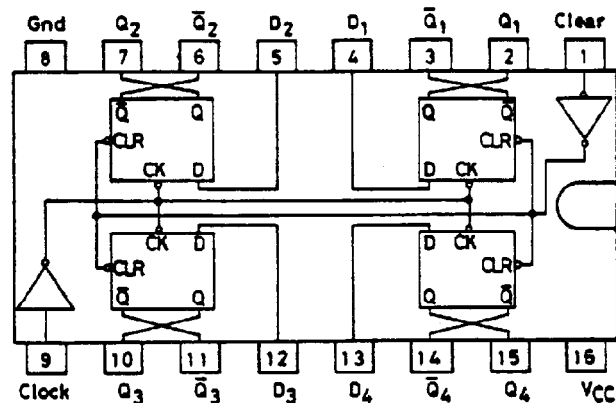
X = Irrelevant.

$\uparrow$ = Transition from LOW to HIGH level.

Q_0 = The level of Q before the indicated steady-state input conditions were established.

Table II

Logic diagram and connections

**3. Marking**

(1) Each integrated circuit shall bear the following markings:

- Terminal identification.
- The manufacturer's type number.
- The factory identification code.
- The date code.

(2) Each package containing one or more of these circuits shall bear the markings 'b', 'c' and 'd' above and in addition:

- The BS detail specification number e.g., BS 9420 F055.

4. Related documents

BS 3934 'Dimensions of semiconductor devices',

BS 6001 'Sampling procedures and tables for inspection by attributes',

BS 9000 'General requirements for electronic components of assessed quality',

PD 9002 'Qualified products list for electronic components of assessed quality',

BS 9400 'Integrated electronic circuits of assessed quality: Generic data and methods of test'.

5. Ordering information

Manufacturer's integrated circuit type and package identification as detailed in PD 9002 to BS 9420 F... as defined below.

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual in-line and Flat-Pack	54175	F073	F074	F075	F161	F055
	64175	★	F162	F163	F164	F056
	74175	★	F165	F166	F167	F057
PLASTIC Dual in-line	54175	★	★	★	★	F055
	64175	★	★	★	★	F056
	74175	★	★	★	★	F057

★ = Not available at the present time.

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6. Screening procedures

Production batches submitted for 100% screening shall be rejected if more than a total of 10% of the devices in the batch fail the electrical test requirements subsequent to the burn-in screen 1.2.9.2 in categories S1, S2 and S4.

