

UTE

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CECC 90 101-055

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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
*ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :*

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 75

Adoptée le 16 novembre 1987

BS9440 F0744 to F0756

Issue 1

August, 1980

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 09 - 050 G 08
IEC 191-2 - Types 050 G 09 - 050 G 08

Référence française : F 117 - F 117A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS IN ACCORDANCE WITH FS 90 101

54/64/74 179

**REGISTRE A DECALAGE
A ENTREES PARALLELES**

**4-BIT PARALLEL ACCESS
SHIFT REGISTER**

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

*Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.*

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :

AMENDMENTS TO THE FOLLOWING CLAUSES

§ 2 - Add :

Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$

§ 3 To be replaced by CECC 90 000/3 § 2.5

§ 4 To be deleted

§ 5 To be replaced by CECC 90 000/3 § 2.6

§ 6 To be replaced by CECC 90 000/3 § 4.10.1

§ 7 All inspection level and AQL are those specified in 90 100/3.

Replace A3b by A4a, A3c by A4b, A4 by A5.

Add A8 of 90 100/3 (Assessment level P only).

Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.

For groups B, C, D, apply 90 100/3.

Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

BRITISH STANDARDS INSTITUTION

2, PARK STREET, LONDON, W1A 2BS

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ELECTRONIC COMPONENTS OF ASSESSED QUALITY

DETAIL SPECIFICATION IN ACCORDANCE WITH
BS 9400: 1970

MANUFACTURER'S TYPE NUMBER

54179

64179

74179

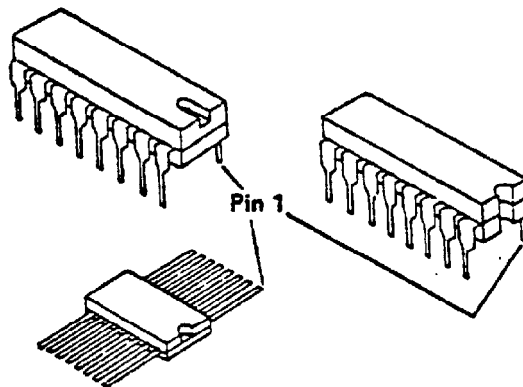
SEE PD 9002

For ordering information
see clause 5.SILICON MONOLITHIC TTL
4-BIT PARALLEL ACCESS
SHIFT REGISTER

(see Clause 8)

CERAMIC/GLASS HERMETICALLY
SEALED ENCAPSULATION OR
DUAL-IN-LINE PLASTIC
ENCAPSULATIONFULL ASSESSMENT LEVEL AND
APPLICATION CATEGORIES
S1, S2, S3 and S4

Outline not to scale. Isometric projection.



For detail dimensions:

- Lead Flatpack — See Appendix 1
- Lead Dual-in-line — BS 3934 SO-87C
- Marking information — See Clause 3

1. LIMITING CONDITIONS OF USE (not for inspection purposes)

Absolute values (non-simultaneous)

V_{CC}	Maximum continuous positive supply voltage	7.0 V
	Maximum continuous negative supply voltage	0.5 V
V_{IN}	Maximum continuous positive input voltage	5.5 V
$-V_{IN}$	Maximum continuous negative input voltage	0.5 V
$-I_{IN}$	Maximum input current (clamping mode)	12.0 V
T_{amb}	Ambient operating temperature range	-55°C to +125°C -40°C to + 85°C 0°C to + 70°C
T_{stg}	Storage temperature range	-65°C to +150°C
	Shock (0.5 ms duration)	14 700 m/s ²
	Vibration	196 m/s ²

Refer to Qualified Products List PD 9002 for details of manufacturers approved to this specification

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2. Recommended Conditions of Use and Associated Characteristics
(not for inspection purposes)

These characteristics apply over the ambient operating temperature range unless otherwise stated.

			<u>Min.</u>	<u>Max.</u>	<u>Unit</u>
V_{CC}	Positive supply voltage	54179	4.5	5.5	V
		64179, 74179	4.75	5.25	V
I_{CC}	Total supply current per package at V_{CC} maximum	54179	-	70.0	mA
		64179, 74179	-	75.0	mA
V_{IH}	HIGH state input voltage		2.0	5.5	V
V_{IL}	LOW state input voltage		-	0.8	V
V_{OH}	HIGH state output voltage at $-I_{OH} = I_{OH} \text{ max.}$		2.4	-	V
V_{OL}	LOW state output voltage $I_{OL} = I_{OL} \text{ max.}$		-	0.4	V
$I_{IH(1)}$	HIGH state input current $V_{IN} = V_{IH} \text{ max.}$		-	1.0	mA
$I_{IH(2)}$	HIGH state input current $V_{IN} = V_{OH} \text{ min.}$		-	40.0	μ A
$-I_{IL}$	LOW state input current $V_{IN} = V_{OL} \text{ max.}$		-	1.6	mA
$-I_{OH}$	HIGH state output current		-	0.8	mA
I_{OL}	LOW state output current		-	16.0	mA
$-I_{OS}$	Output short circuit current				
		54179	20.0	57.0	mA
		64179, 74179	18.0	57.0	mA
$-V_{IK}$	Input clamping voltage $-I_1 = 12\text{mA}$		-	1.5	V

2. Recommended Conditions of Use and Associated Characteristics (Cont'd)

= Switching Characteristics
 $V_{CC} = 5V$, $T_{amb} = 25^{\circ}C$, $C_L = 15\text{ pF}$, $R_L = 400\Omega$

		<u>Min.</u>	<u>Max.</u>	<u>Unit</u>
t_{PHL}	HIGH to LOW state propagation time			
	From clear to Q_A , Q_B , Q_C , Q_D	-	36.0	ns
	From clock to any output	-	35.0	ns
t_{PLH}	LOW to HIGH state propagation time			
	From clear to $\overline{Q}_D$	-	23.0	ns
	From clock to any output	-	26.0	ns
$f_{max.}$	Maximum clock frequency	25.0	-	MHz
$t_{p(clock)}$	Width of clock pulse	20.0	-	ns
$t_{p(clear)}$	Width of clear pulse	20.0	-	ns
t_{set-up}	Input set-up time			
	Shift (H or L) or load	35.0	-	ns
	Data	30.0	-	ns
	Clear-inactive-state	15.0	-	ns
t_{hold}	Input hold time	5.0	-	ns

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FUNCTION TABLETABLE I

INPUTS					OUTPUTS								
CLEAR ¹	SHIFT	LOAD	CLOCK	SERIAL	PARALLEL				Q _A	Q _B	Q _C	Q _D	Q _D [†]
					A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	X	X	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
H	L	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
H	L	H	X	X	a	b	c	d	a	b	c	d	a
H	H	X	X	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}
H	H	X	X	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}

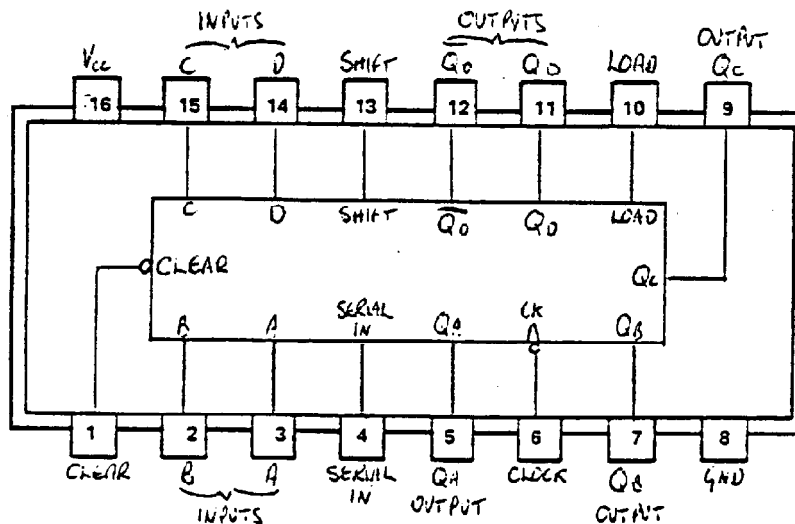
[†] The columns for clear, Q_D, and the top line of the table apply for the 179 only.

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input including transitions)

L = transition from high to low level

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most recent transition of the clockPIN CONNECTION DIAGRAMTABLE II

3. MARKING.

3.1 Each integrated circuit shall bear the following markings:

- (a) Terminal identification.
- (b) The manufacturer's type number.
- (c) The factory identification code, or manufacturer's trade mark.
- (d) The date code.

3.2 Each package containing one or more of these circuits shall bear the markings (b), (c) and (d) above and in addition:

- (e) The B.S. detail specification number.

4. RELATED DOCUMENTS.

BS 2011 Basic environmental testing procedures.

BS 3934 Dimensions of semiconductor devices.

BS 6001 Sampling procedures and tables for inspection by attributes.

BS 9000 General requirements for electronic components of assessed quality.

BS 9400 Integrated electronic circuits of assessed quality: Generic data and methods of test.

PD 9002 Qualified Products List for electronic components of assessed quality.

5. ORDERING INFORMATION.

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification
as detailed in PD 9002 to BS9440 F..... as defined below -

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual-in-line and Flatpack	54179	F0744	F0745	F0746	F0747	F0748
	64179	*	F0749	F0750	F0751	F0752
	74179	*	F0753	F0754	F0755	F0756
PLASTIC Dual-in-line	54179	*	*	*	*	F0748
	64179	*	*	*	*	F0752
	74179	*	*	*	*	F0756

Note: * Not available at present.