

UTE

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CECC 90 101-057

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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
*ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :*

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 77

Adoptée le 16 novembre 1987

BS9440 F0783 to F0795

Issue 1

February, 1981

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 051 G 01 - 051 G 02

IEC 191-2 - Types 051 G 01 - 051 G 02

ou/or

Boîtier identique mais avec : $e_1 = 7,62 \text{ mm}$ Same package but with : $e_1 = 0,300"$

Référence française : Néant

French reference : None

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II

See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
*DETAIL SPECIFICATION FOR DIGITAL INTEGRATED
CIRCUITS IN ACCORDANCE WITH FS 90 101*

54/64/74 199**REGISTRE A DECALAGE A ENTREES PARALLELES**

**SHIFT REGISTER WITH PARALLEL LOAD,
SHIFT (Q_A TOWARD Q_H),
SERIAL $\bar{J}$ - $\bar{K}$ INPUTS AND INHIBIT CLOCK**

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers avec ou sans cavité.

Silicon monolithic bipolar integrated circuit, cavity/non-cavity packages.

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L.
ASSESSMENT LEVELS :

AMENDMENTS TO THE FOLLOWING CLAUSES

§ 2 - Add :

Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$

§ 3 To be replaced by CECC 90 000/3 § 2.5

§ 4 To be deleted

§ 5 To be replaced by CECC 90 000/3 § 2.6

§ 6 To be replaced by CECC 90 000/3 § 4.10.1

§ 7 All inspection level and AQL are those specified in 90 100/3.

Replace A3b by A4a, A3c by A4b, A4 by A5.

Add A8 of 90 100/3 (Assessment level P only).

Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.

For groups B, C, D, apply 90 100/3.

Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

BRITISH STANDARDS INSTITUTION

2, PARK STREET, LONDON, W1A 2BS

Specification available from:— As shown in PD 9002

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**ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH**

BS9400: 1970

MANUFACTURER'S TYPE NUMBER

54199

64199

74199

See PD 9002

For ordering information

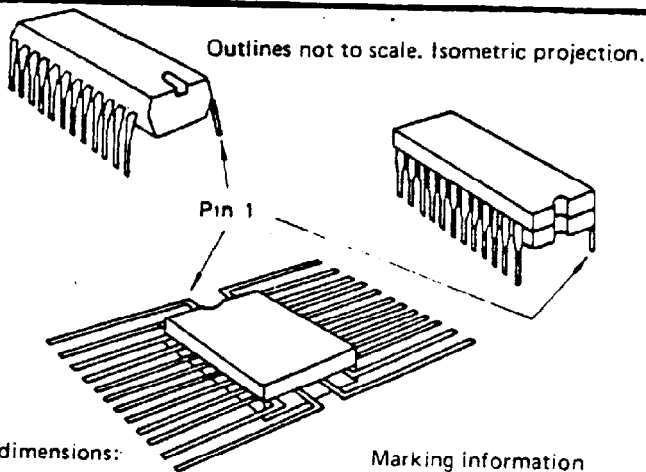
see Clause 5

SILICON MONOLITHIC TTL 8-BIT
SHIFT REGISTER WITH PARALLEL
LOAD, SHIFT (QA TOWARD QH),
SERIAL J-K INPUTS AND INHIBIT
CLOCK (See Clause 8)

CERAMIC/GLASS HERMETICALLY
SEALED ENCAPSULATION OR
DUAL-IN-LINE PLASTIC
ENCAPSULATION

**FULL ASSESSMENT LEVEL AND
APPLICATION CATEGORIES**

S1, S2, S3 and S4



For details dimensions:

24 lead flat-pack — see Appendix I

24 lead Dual-in-line — see BS 3934, SO-120B

Marking information
see Clause 3**1. LIMITING CONDITIONS OF USE (not for inspection purposes)**

Absolute values (non-simultaneous)

V_{CC}	Maximum continuous positive supply voltage		7.0 V
	Maximum continuous negative supply voltage		0.5 V
V_{IN}	Maximum continuous positive input voltage		5.5 V
	Maximum continuous negative input voltage (non-clamping mode)		0.5 V
$-I_{IN}$	Maximum negative input current (clamping mode)		12.0 mA
	Maximum reverse input current		1.0 mA
T_{amb}	Ambient operating temperature range	54199	-55 °C to +125 °C
		64199	-40 °C to + 85 °C
		74199	0 °C to + 70 °C
T_{stg}	Storage temperature range		-65 °C to +150 °C
	Shock (0.5 ms duration)		14 700 m/s ²
	Vibration		196 m/s ²

Refer to Qualified Products List PD 9002 for details of Manufacturers.
approved to this specification

2. Recommended Conditions of Use and Associated Characteristics (Not for inspection purposes)

These characteristics apply over the ambient operating temperature range unless otherwise stated.

			<u>Min.</u>	<u>Max.</u>	<u>Unit</u>
V_{CC}	Positive supply voltage	54199	4.5	5.5	V
		64199, 74199	4.75	5.25	V
I_{CC}	Total supply current per package at V_{CC} maximum.				
	Outputs High		-	127.0	mA
V_{IH}	HIGH state input voltage		2.0	5.5	V
V_{IL}	LOW state input voltage		-0.3	0.8	V
V_{OH}	HIGH state output voltage at $-I_{OH} = I_{OH}$ max.		2.4	-	V
V_{OL}	LOW state output voltage $I_{OL} = 16$ mA		-	0.4	V
$I_{IH(1)}$	HIGH state input current $V_{IN} = V_{IH}$ max.		-	1.0	mA
$I_{IH(2)}$	HIGH state input current $V_{IN} = V_{OH}$ min.		-	40.0	μ A
$-I_{IL}$	LOW state input current $V_{IN} = V_{OL}$ max.		-	1.6	mA
$-I_{OH}$	HIGH state output current		-	800.0	μ A
I_{OL}	LOW state output current		-	16.0	mA
$-I_{OS}$	Output short circuit current				
		54199	20.0	57.0	mA
		64199, 74199	18.0	57.0	mA
$-V_{IC}$	Input clamping voltage $-I_{IN} = 12$ mA		-	1.5	V

2. Recommended Conditions of Use and Associated Characteristics (Cont'd)Switching Characteristics
 $V_{CC} = 5 \text{ V}$, $T_{amb} = 25^{\circ}\text{C}$, $C_L = 15 \text{ pF}$, $R_L = 400\Omega$

		<u>Min.</u>	<u>Max.</u>	<u>Unit</u>
t_{PHL}	HIGH to LOW state propagation time			
	From Clock to Output	-	30.0	ns
	From Clear to Output	-	35.0	ns
t_{PLH}	LOW to HIGH state propagation time			
	From Clock to Output	-	26.0	ns
f_{CLOCK}	Clock Frequency	0	25.0	MHz
t_{su}	Set up time Mode Control	30.0	-	ns
	Data	20.0	-	ns
t_w	Hold time at any input	0	-	ns
t_w	Width of clock or clear pulse	20.0	-	ns

FUNCTION TABLETABLE I

INPUTS						OUTPUTS			
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL J K	PARALLEL A...H	Q _A	Q _B	Q _C	... Q _H
L	X	X	X	X X	X	L	L	L	L
H	X	L	L	X X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{H0}
H	L	L	↑	X X	a...h	a	b	c	h
H	H	L	↑	L H	X	Q _{A0}	Q _{A0}	Q _{Bn}	Q _{Gn}
H	H	L	↑	L L	X	L	Q _{An}	Q _{Bn}	Q _{Gn}
H	H	L	↑	H H	X	H	Q _{An}	Q _{Bn}	Q _{Gn}
H	H	L	↑	H L	X	Q _{An}	Q _{An}	Q _{Bn}	Q _{Gn}
H	X	H	↑	X X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{H0}

H = high level (steady state), L = low level (steady state)

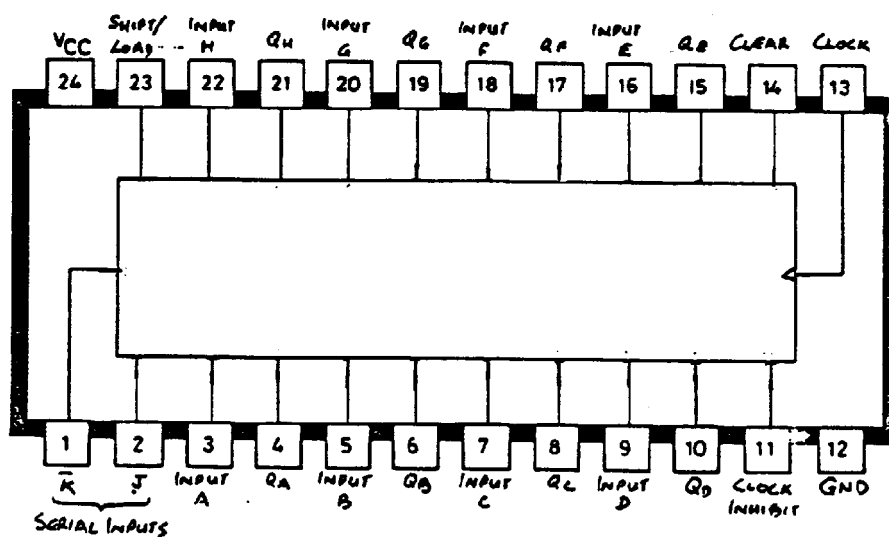
X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a...h = the level of steady-state input at inputs A thru H, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, ... Q_{H0} = the level of Q_A, Q_B, or Q_C thru Q_H, respectively, before the indicated steady-state input conditions were established.Q_{An}, Q_{Bn}, ... Q_{Gn} = the level of Q_A or Q_B thru Q_G, respectively, before the most-recent ↑ transition of the clock.

SEE FIG. 3 FOR TYPICAL OPERATING SEQUENCE.

PIN CONNECTION DIAGRAMTABLE II

3. MARKING.

3.1 Each integrated circuit shall bear the following markings:

- (a) Terminal identification.
- (b) The manufacturer's type number.
- (c) The factory identification code, or manufacturer's trade mark.
- (d) The date code.

3.2 Each package containing one or more of these circuits shall bear the markings (b), (c) and (d) above and in addition:

- (e) The B.S. detail specification number.

4. RELATED DOCUMENTS.

BS 2011 Basic environmental testing procedures.

BS 3934 Dimensions of semiconductor devices.

BS 6001 Sampling procedures and tables for inspection by attributes.

BS 9000 General requirements for electronic components of assessed quality.

BS 9400 Integrated electronic circuits of assessed quality: Generic data and methods of test.

PD 9002 Qualified Products List for electronic components of assessed quality.

5. ORDERING INFORMATION.

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification
as detailed in PD 9002 to BS 9440 F..... as defined below -

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual-in-line and Flatpack	54199	F0783	F0784	F0785	F0786	F0787
	64199	*	F0788	F0789	F0790	F0791
	74199	*	F0792	F0793	F0794	F0795
PLASTIC Dual-in-line		*	*	*	*	
	64199	*	*	*	*	F0791
	74199	*	*	*	*	F0795

Note: * Not available at present.