

UTE

Spécification française harmonisée
Système CENELEC d'assurance de la qualité

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CECC 90 101-059

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Page 0

Nombre total de pages : 19
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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
*ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :*

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 79

Adoptée le 16 novembre 1987

BS9490 F6308 to F6320

Issue 1
October, 1980

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 09 - 050 G 08
IEC 191-2 - Types 050 G 09 - 050 G 08

Référence française : F 117 - F 117A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
*DETAIL SPECIFICATION FOR DIGITAL INTEGRATED
CIRCUITS IN ACCORDANCE WITH FS 90 101*

54/64/74 365A

AMPLIFICATEUR DE BUS
A SORTIES 3 ETATS DE PUISSANCE

**HEX BUFFER DRIVERS
WITH 3-STATE OUTPUTS**

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

*Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.*

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :

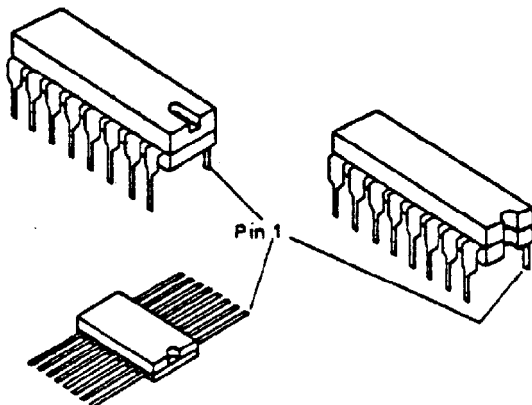
AMENDMENTS TO THE FOLLOWING CLAUSES

- § 2 - Add :
Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$
- § 3 To be replaced by CECC 90 000/3 § 2.5
- § 4 To be deleted
- § 5 To be replaced by CECC 90 000/3 § 2.6
- § 6 To be replaced by CECC 90 000/3 § 4.10.1
- § 7 All inspection level and AQL are those specified in 90 100/3.
*Replace A3b by A4a, A3c by A4b, A4 by A5.
Add A8 of 90 100/3 (Assessment level P only).
Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.
For groups B, C, D, apply 90 100/3.
Sub-groups A6, A7 : not applicable.*

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.
Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON, W1A 2BS		BS9490 F6308 to F6320 ISSUE 1 OCTOBER 1980	
Specification available from:— As shown in PD 9002 and:— TEXAS INSTRUMENTS LIMITED, MANTON LANE, BEDFORD, MK41 7PA		Page 1 of 18 Pages	
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH BS9400 : Issue 2		MANUFACTURER'S TYPE NUMBER 54365A 64365A 74365A	
Outlines not to scale. Isometric projection. 		For ordering information see Clause 5 SILICON MONOLITHIC TTL HEX BUFFER DRIVERS WITH THREE- STATE OUTPUTS (See Clause 8)	
For details dimensions: 16 Lead Flat-Pack — see Appendix I 16 Lead Dual in-line — see BS 3934 SO-87C		CERAMIC/GLASS HERMETICALLY SEALED ENCAPSULATION OR DUAL-IN-LINE PLASTIC ENCAPSULATION FULL ASSESSMENT LEVEL AND APPLICATION CATEGORIES S1, S2, S3 AND S4	
Marking information see Clause 3			

1. LIMITING CONDITIONS OF USE (not for inspection purposes)

Absolute values (non-simultaneous)

V_{CC}	Maximum continuous positive supply voltage	7.0	V
	Maximum continuous negative supply voltage	0.5	V
	Maximum continuous positive input voltage	5.5	V
	Maximum continuous negative input voltage (non-clamping mode)	0.5	V
	Maximum negative input current (clamping mode)	12.0	mA
	Maximum reverse input current	1.0	mA
T_{amb}	Ambient operating temperature range	54365A	-55 to +125 °C
		64365A	-40 to +85 °C
		74365A	0 to +70 °C
T_{stg}	Storage temperature range	-65	to +150 °C
	Shock (0.5 ms duration)	14 700	m/s ²
	Vibration	196	m/s ²

Refer to Qualified Products List PD 9002 for details of Manufacturers approved to this specification

BS9490 F6308 to F6320
 ISSUE 1
 OCTOBER 1980

2. RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS
 (not for inspection purposes)

These characteristics apply over the full temperature range unless otherwise stated.

		Min.	Max.	Unit
V_{CC}	Positive supply voltage 54365A	4.5	5.5	V
	64365A, 74365A	4.75	5.25	V
V_{IH}	HIGH state input voltage	2.0	5.5	V
I_{CC}	Total supply current per package at V_{CC} maximum value	-	85.0	mA
V_{OH}	HIGH state output voltage at V_{CC} minimum value	2.4	-	V
$-I_{OLZ}$	High impedance state output current $V_{OUT} = 0.4V$	-	40.0	μA
I_{OHZ}	High impedance state output current $V_{OUT} = 2.4V$	-	40.0	μA
V_{IL}	LOW state input voltage	0.3	0.8	V
V_{OL}	LOW state output voltage at $V_{CC} =$ minimum value	-	0.4	V
$-V_{IC}$	Input clamping voltage at $V_{CC} =$ minimum value $-I_{IN} = 12$ mA	-	1.5	V
$I_{IH(1)}$	HIGH state input current at $V_{CC} =$ maximum value $V_{IN} = 7.0V$	-	1.0	mA
$I_{IH(2)}$	HIGH state input current $V_{IN} = 2.7V$	-	40.0	μA
$-I_{IL}$	LOW state input current at $V_{CC} =$ maximum value			
	$V_{IN} = 0.5V$ (either G inputs at 2V) A Input		40.0	μA
	$V_{IN} = 0.4V$ (either G inputs at 0.4V) A Input		1.6	mA
	$V_{IN} = V_{OL}$ maximum		1.6	mA

2. RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS
(Continued)

		<u>Min.</u>	<u>Max.</u>	<u>Unit</u>
$-I_{OH}$	HIGH state output current			
	54365A	-	2.0	mA
	64365A, 74365A	-	5.2	mA
I_{OL}	LOW state output current	-	32.0	mA
$-I_{OS}$	Short circuit output current	40.0	130.0	mA

Switching Characteristics

$V_{CC} = 5V$, $T_{amb} = 25^{\circ}C$, $C_L = 45 \text{ pF}$, $R_L = 667\Omega$

t_{PLH}	Propagation delay time LOW to HIGH state	-	16.0	ns
t_{PHL}	Propagation delay time HIGH to LOW state	-	22.0	ns
t_{PZH}	Propagation delay time Output enable to HIGH level	-	35.0	ns
t_{PZL}	Propagation delay time Output enable to LOW level	-	37.0	ns
t_{PHZ}	Propagation delay time Output disable from HIGH level	-	11.0	ns
	$C_L = 5\text{pF}$, $R_L = 667\Omega$			
t_{PLZ}	Propagation delay time Output disable from LOW level	-	27.0	ns
	$C_L = 5\text{pF}$, $R_L = 667\Omega$			

BS9490 F6308 to F6320
ISSUE 1
OCTOBER 1980

TABLE I

LOGIC FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

H = HIGH state

L = LOW state

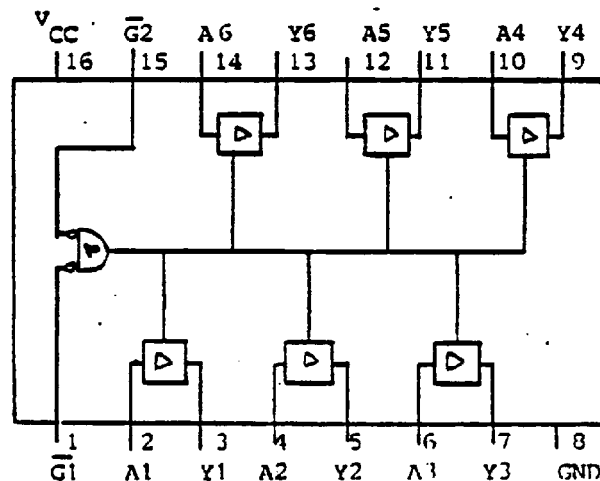
X = Logic state irrelevant

Z = High impedance state (output disabled) - See Clause 8

G_1 & G_2 disable inputs

TABLE II

CONNECTION DIAGRAM



3. MARKING.

3.1 Each integrated circuit shall bear the following markings:

- (a) Terminal identification.
- (b) The manufacturer's type number.
- (c) The factory identification code, or manufacturer's trade mark.
- (d) The date code.

3.2 Each package containing one or more of these circuits shall bear the markings (b), (c) and (d) above and in addition:

- (e) The B.S. detail specification number.

4. RELATED DOCUMENTS.

BS 2011 Basic environmental testing procedures.

BS 3934 Dimensions of semiconductor devices.

BS 6001 Sampling procedures and tables for inspection by attributes.

BS 9000 General requirements for electronic components of assessed quality.

BS 9400 Integrated electronic circuits of assessed quality: Generic data and methods of test.

PD 9002 Qualified Products List for electronic components of assessed quality.

5. ORDERING INFORMATION.

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification
as detailed in PD 9002 to BS9490 F..... as defined below -

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual-in-line and Flatpack	54365A	F6308	F6309	F6310	F6311	F6312
	64365A	*	F6313	F6314	F6315	F6316
	74365A	*	F6317	F6318	F6319	F6320
PLASTIC Dual-in-line	54365A	*	*	*	*	F6312
	64365A	*	*	*	*	F6316
	74365A	*	*	*	*	F6320

Note: * Not available at present.