

UTE

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CECC 90 101-061

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Page 0

Nombre total de pages : 19
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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 81

Adoptée le 16 novembre 1987

BS9403 F0262 to F0274

Issue 1

May, 1982

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 09 - 050 G 08
IEC 191-2 - Types 050 G 09 - 050 G 08

Référence française : F 117 - F 117A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED
CIRCUITS IN ACCORDANCE WITH FS 90 101

54/64/74 368A

AMPLIFICATEUR DE BUS A SORTIES
3 ETATS DE PUISSANCE

BUS DRIVER WITH 3 STATE OUTPUTS

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :

AMENDMENTS TO THE FOLLOWING CLAUSES

§ 2 - Add :

Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$

Page 3, switching characteristics, replace $C_L = 45 \text{ pF}$ and $R_L = 667 \Omega$ by $C_L = 50 \text{ pF}$ and $R_L = 400 \Omega$

§ 3 To be replaced by CECC 90 000/3 § 2.5

§ 4 To be deleted

§ 5 To be replaced by CECC 90 000/3 § 2.6

§ 6 To be replaced by CECC 90 000/3 § 4.10.1

§ 7 All inspection level and AQL are those specified in 90 100/3.

Page 10, switching characteristics, replace $C_L = 45 \text{ pF}$ and $R_L = 667 \Omega$ by $C_L = 50 \text{ pF}$ and $R_L = 400 \Omega$

Page 10, t_{PHZ} parameter : replace limit 16 ns by 11 ns

Replace A3b by A4a, A3c by A4b, A4 by A5.

Add A8 of 90 100/3 (Assessment level P only).

Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.

For groups B, C, D, apply 90 100/3.

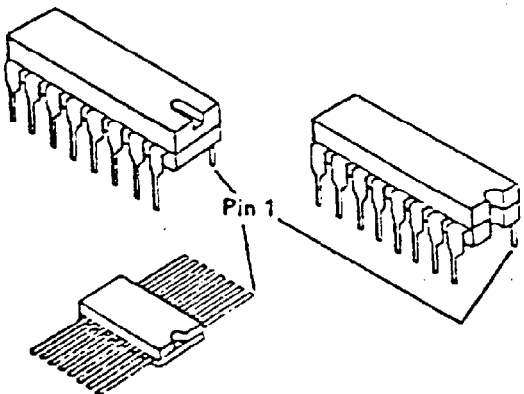
Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current
CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON, W1A 2BS Specification available from:— As shown in PD 9002	BS9403 FO262 to FO274 ISSUE 1 MAY 1982 Page 1 of 18 Pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH BS 9400 : 1970	MANUFACTURER'S TYPE NUMBER 54368A 64368A 74368A
Outline not to scale. Isometric projection.  For detail dimensions: Lead Flatpack — See Appendix 1 Lead Dual-in-line — BS 3934 SO-87B Marking information — See Clause 3	SEE PD 9002 For ordering information see Clause 5 SILICON MONOLITHIC TTL HEX BUS DRIVER WITH 3-STATE OUTPUTS (SEE CLAUSE 8) CERAMIC/GLASS HERMETICALLY SEALED ENCAPSULATION OR DUAL-IN-LINE PLASTIC ENCAPSULATION FULL ASSESSMENT LEVEL AND APPLICATION CATEGORIES S1, S2, S3 AND S4

1. LIMITING CONDITIONS OF USE (not for inspection purposes)

Absolute values (non-simultaneous)

V_{CC}	Maximum continuous positive supply voltage	7.0	V
	Maximum continuous negative supply voltage	0.5	V
V_{IN}	Maximum continuous positive input voltage	5.5	V
$-V_{IN}$	Maximum continuous negative input voltage	0.5	V
$-I_{IN}$	Maximum input current (clamping mode)	12.0	mA
	Maximum reverse input current	1.0	mA
T_{amb}	Ambient operating temperature range	54368A	-55 °C to +125 °C
		64368A	-40 °C to +85 °C
		74368A	0 °C to +70 °C
T_{stg}	Storage temperature range	-65 °C to +150 °C	
	Shock (0.5 ms duration)	14 700	m/s ²
	Vibration	196	m/s ²

Refer to Qualified Products List PD 9002 for details of Manufacturers approved to this specification

2. RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS (Cont'd) (not for inspection purposes)

These characteristics apply over the ambient operating temperature range unless otherwise stated.

			<u>Min.</u>	<u>Max.</u>	<u>Unit</u>
V_{CC}	Positive supply voltage	54368A	4.5	5.5	V
		64368A & 74368A	4.75	5.25	V
I_{CC}	Total supply current per package at V_{CC} maximum.				
	All inputs at 0V				
	Control inputs at 4.5V		-	77.0	mA
V_{IH}	HIGH state input voltage		2.0	5.5	V
V_{IL}	LOW state input voltage		-0.3	0.8	V
V_{OH}	HIGH state output voltage at V_{CC} minimum		2.4	-	V
V_{OL}	LOW state output voltage				
	$I_{OL} = 32.0$ mA		-	0.4	V
$-V_{IC}$	Input clamping voltage at		-	1.5	V
	$-I_{IN} = 12.0$ mA				
$I_{IH(1)}$	HIGH state input current		-	1.0	mA
	$V_{IN} = V_{IH}$ max.				
$I_{IH(2)}$	HIGH state input current		-	40.0	μ A
	$V_{IN} = V_{OH}$ min.				
$-I_{IL}$	LOW state input current				
	$V_{IN} = V_{OL}$ max.				
	Outputs disabled		-	40.0	μ A
	Outputs enabled		-	1.6	mA
$-I_{OH}$	HIGH state output current				
		54368A	-	2.0	mA
		64368A & 74368A	-	5.2	mA
I_{OL}	LOW state output current		-	32.0	mA
I_{OHZ}	High impedance state output current		-	40.0	μ A
	$V_{OUT} = 2.4$ V				

2. RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS (Cont'd)
(not for inspection purposes)

		<u>Min.</u>	<u>Max.</u>	<u>Unit</u>
$-I_{OLZ}$	High impedance state output current $V_{OUT} = 0.4V$	-	40.0	μA
$-I_{OS}$	Short circuit output current	40.0	130.0	mA

Switching Characteristics $V_{CC} = 5V$, $T_{amb} = 25^{\circ}C$, $C_L = 45pF$, $R_L = 667\Omega$

t_{PLH}	LOW to HIGH state propagation delay time	-	17.0	ns
t_{PHL}	HIGH to LOW state propagation delay time	-	16.0	ns
t_{PZH}	High impedance to HIGH state (output enable)	-	35.0	ns
t_{PZL}	High impedance to LOW state	-	37.0	ns
t_{PHZ}	HIGH state to high impedance (output disable) ($C_L = 5pF$)	-	11.0	ns
t_{PLZ}	LOW state to high impedance (output disable) ($C_L = 5pF$)	-	27.0	ns

TABLE 1

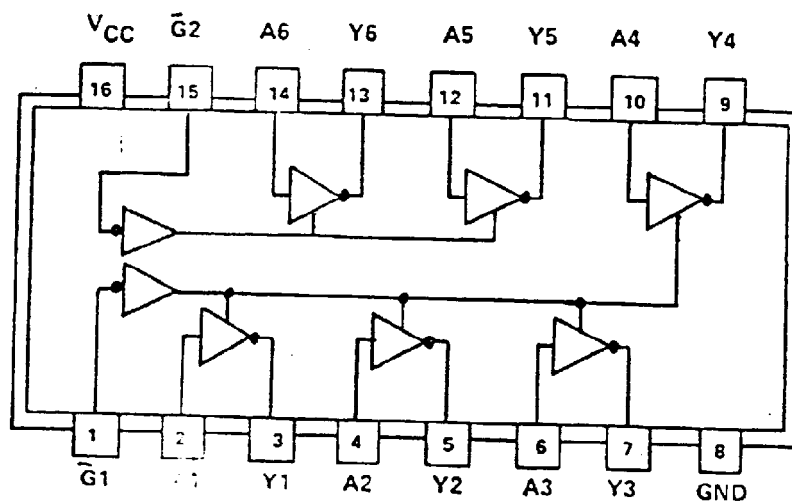
FUNCTION TABLE

INPUTS		OUTPUTS
G	A	Y
H	X	Z
L	H	L
L	L	H

H = HIGH state
L = LOW state
X = Logic state irrelevant
Z = High impedance state

TABLE II

PIN CONNECTION DIAGRAM



3. MARKING.

3.1 Each integrated circuit shall bear the following markings:

- (a) Terminal identification.
- (b) The manufacturer's type number.
- (c) The factory identification code, or manufacturer's trade mark.
- (d) The date code.

3.2 Each package containing one or more of these circuits shall bear the markings (b), (c) and (d) above and in addition:

- (e) The B.S. detail specification number.

4. RELATED DOCUMENTS.

- BS 2011 Basic environmental testing procedures.
- BS 3934 Dimensions of semiconductor devices.
- BS 6001 Sampling procedures and tables for inspection by attributes.
- BS 9000 General requirements for electronic components of assessed quality.
- BS 9400 Integrated electronic circuits of assessed quality: Generic data and methods of test.
- PD 9002 Qualified Products List for electronic components of assessed quality.

5. ORDERING INFORMATION.

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification
as detailed in PD 9002 to BS9403 F..... as defined below -

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual-in-line and Flatpack	54368A	FO262	FO263	FO264	FO265	FO266
	64368A	•	FO267	FO268	FO269	FO270
	74368A	•	FO271	FO272	FO273	FO274
PLASTIC Dual-in-line	54368A	•	•	•	•	FO266
	64368A	•	•	•	•	FO270
	74368A	•	•	•	•	FO274

Note: • Not available at present.