

**BRITISH STANDARDS INSTITUTION**

2 PARK STREET, LONDON. W1A 2BS

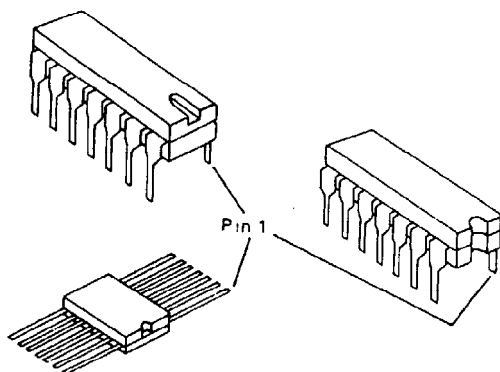
BS CECC 90102 - 008

ISSUE 1

NOVEMBER 1981



Page 1 of 16 pages

**ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:**BS CECC 90 000 : 1976
BS CECC 90 100 : 1977**MANUFACTURERS TYPE NUMBER**54S38
64S38
74S38
84S38Outline not to scale: Isometric projection
Marking information see clause 1Refer to IEC 191-1-50a (type A50B)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1**QUADRUPLE 2-INPUT POSITIVE
NAND BUFFERS WITH OPEN
COLLECTOR OUTPUTS**TYPICAL CONSTRUCTION
SILICON MONOLITHIC BIPOLAR
CAVITY AND NON-CAVITY
PACKAGESASSESSMENT LEVELS
R, S, T, AND V1. Type description

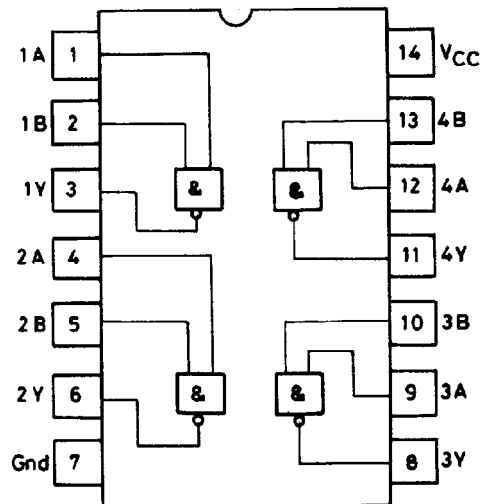
1.1 Truth table

INPUTS		OUTPUT
A	B	Y
H	H	L
L	H	H
H	L	H
L	L	H

H = High level
L = Low levelRefer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Quadruple 2-input positive Nand buffers with open collector outputs

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S38J	N	W
-25 + 85	84S38J		
-40 + 85	64S38J		
-55 +125	54S38J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Minimum and maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Minimum and maximum input voltages							
2.2.1	Minimum and maximum input voltage	V_I						-0,5V +5,5V
				54S	64S	74S	84S	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	0	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Maximum value of Low level output current for each output	I_{OLA}	All types	60,0	mA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54S 64/74/84S	0,3 0,5 0,7	V V V
Maximum applied off-level voltage	V_{OZA}	All types	5,5	V

3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

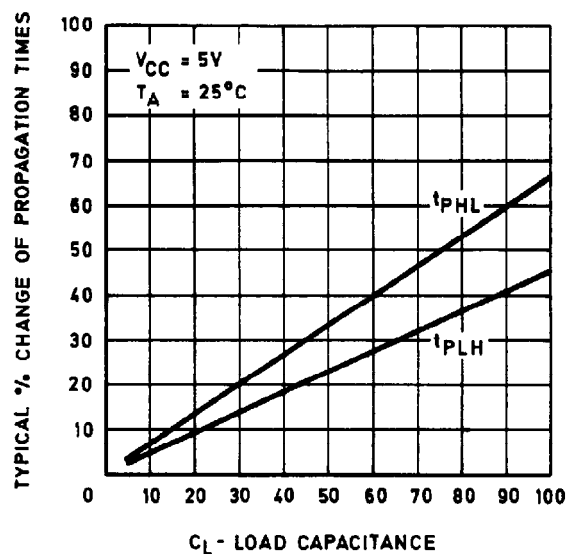
Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current at High level	$V_{IN}^{(1)}$ to give High level output	$V_{CC} \text{ max.}$	I_{CCH}	-	36,0	mA
Total supply current at Low level	$V_{IN}^{(2)}$ to give Low level output	$V_{CC} \text{ max.}$	I_{CCL}	-	80,0	mA
High level input current	$V_{IH(1)} = 5,5V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	1,0	mA
	$V_{IH(2)} = 2,7V$	$V_{CC} \text{ max.}$	$I_{IH(2)}$	-	100,0	μA
Low level input current	$V_{IN} = 0,5V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	4,0	mA
Low level output	$I_{OL} = 60,0mA^{(2)}$	$V_{CC} \text{ min.}$	V_{OL}	-	0,5	V
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{IC}$	-	1,2	V
Propagation times All types	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
High to Low level			t_{PHL}	-	10,0	ns
Low to High level			t_{PLH}	-	10,0	ns

(1) To all inputs (2) Fan out = 30

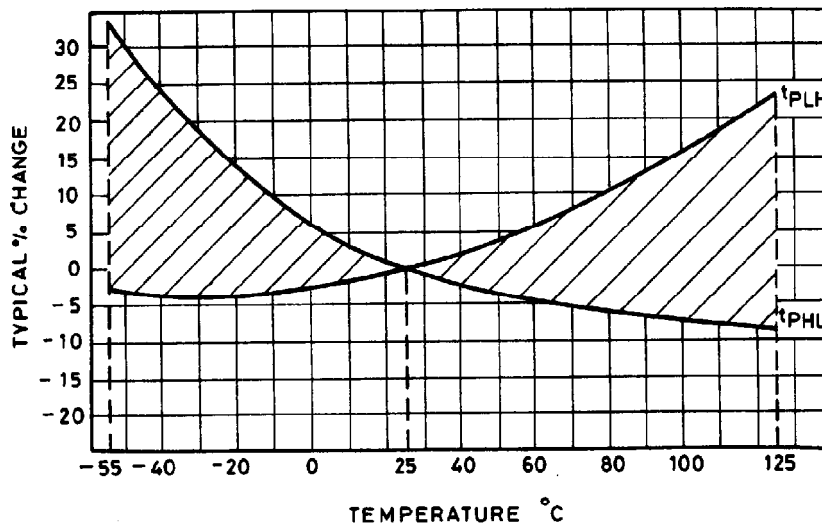
*See Clauses 3.1 and 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



3.3.2 Variation of propagation time with temperature



3.3.3 Gates

Inputs of unused gates should be connected in such a way that the output is set to High level to ensure minimum power dissipation.

For Nand gates unused inputs shall be maintained at a positive voltage $\geq 2,5V$ (54S) or $2,7V$ (64/74/84S), but shall not exceed the absolute maximum rating of $5,5V$.

3.4 Typical values* ($V_{CC} = 5,0V$, $T_{amb} = 25^{\circ}C$)

typical supply current of the device (50% duty cycle)

$$S38 \quad I_{CC} = 8,25mA$$

Typical propagation time:

$$S38 \quad t_{Ptyp} = \frac{t_{PHL} + t_{PLH}}{2} = 6,5ns$$

*See 3.2 of this specification