

BRITISH STANDARDS INSTITUTION, 2 PARK STREET, LONDON, W1A 2BS	Page 1 of 17	CECC 90102 - 019 ISSUE 1 NOVEMBER 1981	
ELECTRONIC COMPONENTS OF ASSESSED QUALITY IN ACCORDANCE WITH: BS CECC 90 000 BS CECC 90 100 and family specification for TTL Schottky-circuits (BS CECC 90102)	BS CECC 90102 - 019 ISSUE 1 NOVEMBER 1981		
Detail specification for 4-2-3-2 input And-Or-invert gates			
Device types: 54S64 64S64 74S64 84S64			
TYPICAL CONSTRUCTION Silicon monolithic bipolar Cavity and non-cavity packages			
Outline and dimensions Refer to IEC 191 1-50a, type A 50 B Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	Assessment levels R, S, T, V		

1. Type description

1.1 Truth table

See relevant Qualified Products List for the availability
of components qualified to this detail specification

1.1 Truth table (contd)

INPUTS											OUTPUT
A	B	C	D	E	F	G	H	I	J	K	Y
H	H	H	H	X	X	X	X	X	X	X	L
X	X	X	X	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
L	L	L	L	L	L	L	L	L	L	L	H

H = High level

L = Low level

X = Logic level irrelevant

NOTE All other combinations not listed above give a High level output

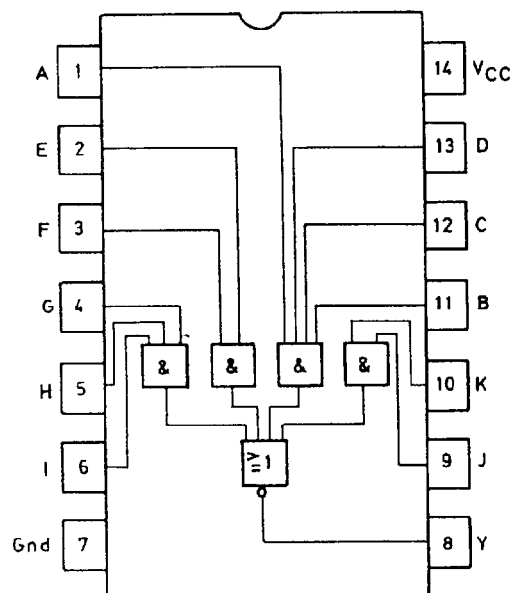
1.1.1 Boolean equation

$$Y \text{ Output} = \overline{ABCD + EF + GHI + JK} \quad (\text{Positive logic})$$

(Inputs)

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



4-2-3-2 input And-Or-invert gates

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S64J	N	W
-25 + 85	84S64J		
-40 + 85	64S64J		
-55 +125	54S64J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

- | | | | |
|-------|--|----------|----------------|
| 2.1 | Minimum and maximum continuous supply voltage | V_{CC} | -0,5V
+7,0V |
| 2.2 | Minimum and maximum input voltages | | |
| 2.2.1 | Minimum and maximum input voltage | V_I | -0,5V
+5,5V |
| 2.2.2 | Maximum input voltage between multiple emitter transistor inputs | V_{II} | +5,5V |

				54S	64S	74S	84S
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	-55	-40	0	-25
			max.	+125	+85	+70	+85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)		
			max.	+150			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	0	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Maximum value of Low level output current for each output	I_{OLA}	All types	20,0	mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	All types	1,0	mA
D.C. noise margin				
at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54S 64/74/84S	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current at High level	V_{IN} to give High level output**	$V_{CC} \text{ max.}$	I_{CCH}	-	12,5	mA
Total supply current at Low level	V_{IN} to give Low level output**	$V_{CC} \text{ max.}$	I_{CCL}	-	16,0	mA
High level input current	$V_{IH(1)} = 5,5V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	1,0	mA
	$V_{IH(2)} = 2,7V$	$V_{CC} \text{ max.}$	$I_{IH(2)}$	-	50,0	μA
Low level input current	$V_{IN} = 0,5V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	2,0	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{IC}$	-	1,2	V
Output voltage	54S $-I_{OH} = 1,0mA$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
	64/74/84S $-I_{OH} = 1,0mA$		V_{OH}	2,7	-	V
	All types $I_{OL} = 20,0mA$ (1)		V_{OL}	-	0,5	V

(1) Fan out = 10,

**Refer to truth table

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output short circuit current	V_{IN} as required to give a High level output $V_O = 0V$ (2)	V_{CC} max.	$-I_{OS}$	40,0	100,0	mA
Propagation times All types	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
High to Low level			t_{PHL}	-	5,5	ns
Low to High level			t_{PLH}	-	5,5	ns

(2) Only one output at a time, duration $t \leq 1$ sec

*See clauses 3.1 and 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading

