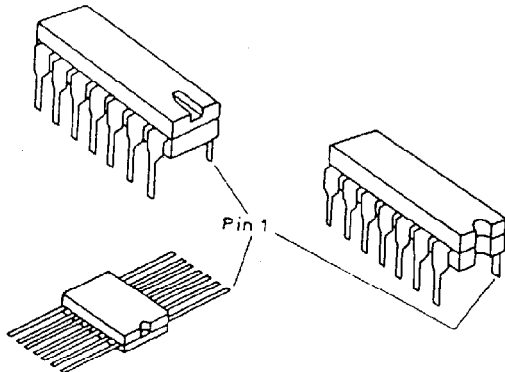




|                                                                                                                                             |                                                                                                                                                                                |
|---------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>BRITISH STANDARDS INSTITUTION</b><br>2 PARK STREET, LONDON. W1A 2BS                                                                      | BS CECC 90102 - 023<br><br>ISSUE 1<br><br>DECEMBER 1981                                                                                                                        |
| Specification available from:- AS SHOWN IN PD 9002<br>AND CECC 00 200 AND                                                                   |                                                                                             |
| ELECTRONIC COMPONENTS OF ASSESSED QUALITY<br>DETAIL SPECIFICATION IN ACCORDANCE WITH:<br><br>BS CECC 90 000 : 1976<br>BS CECC 90 100 : 1977 |                                                                                                                                                                                |
| Outline not to scale: Isometric projection<br>Marking information see clause 1                                                              | Page 1 of 18 pages<br><br>MANUFACTURERS TYPE NUMBER<br><br>54S114<br>64S114<br>74S114<br>84S114<br><br>SEE PD 9002 AND CECC 00 200<br>For ordering information see<br>clause 1 |
|                                                           | DUAL J-K BISTABLES WITH<br>PRESET COMMON CLEAR AND<br>COMMON CLOCK                                                                                                             |
| Refer to IEC 191-1-50a (type A50B)<br>Dual-in-Line (plastic or ceramic)<br>refer to Appendix A1.3<br>Flatpack (metal or ceramic)            | TYPICAL CONSTRUCTION<br>SILICON MONOLITHIC BIPOLAR<br>CAVITY AND NON-CAVITY<br>PACKAGES                                                                                        |
|                                                                                                                                             | ASSESSMENT LEVELS<br>R, S, T, AND V                                                                                                                                            |

1. Type description

## 1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200  
for details of manufacturers approved to this specification

## 1.1 Truth table (contd)

| INPUTS |       |       |   |   | OUTPUTS |             |
|--------|-------|-------|---|---|---------|-------------|
| PRESET | CLEAR | CLOCK | J | K | Q       | $\bar{Q}$   |
| L      | H     | X     | X | X | H       | L           |
| H      | L     | X     | X | X | L       | H           |
| L      | L     | X     | X | X | H*      | H*          |
| H      | H     | ↓     | L | L | $Q_0$   | $\bar{Q}_0$ |
| H      | H     | ↓     | H | L | H       | L           |
| H      | H     | ↓     | L | H | L       | H           |
| H      | H     | ↓     | H | H | TOGGLE  | TOGGLE      |
| H      | H     | H     | X | X | $Q_0$   | $\bar{Q}_0$ |

H = High level

L = Low level

X = Logic level irrelevant

↓ = Transition from High to Low level

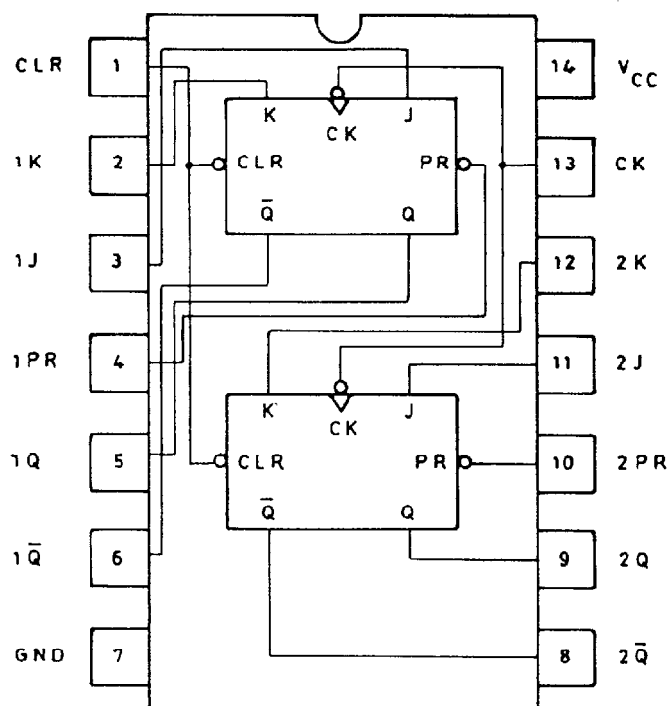
 $Q_0$  = The level of Q before the indicated input conditions were established.

TOGGLE = Each output changes to the complement of its previous level on each active transition of the clock

\* = This configuration is non-stable; i.e. it will not persist when preset and clear inputs return to their inactive level

## 1.2 Terminal identification, type designation and marking

## 1.2.1 Terminal identification



Dual J-K bistables, with preset, common clear and common clock

## 1.2.2 Type designation

| TEMPERATURE<br>RANGE | PACKAGE                 |                         |                     |
|----------------------|-------------------------|-------------------------|---------------------|
|                      | Ceramic<br>Dual-in-Line | Plastic<br>Dual-in-Line | Ceramic<br>Flatpack |
| 0 + 70               | 74S114J                 | N                       | W                   |
| -25 + 85             | 84S114J                 |                         |                     |
| -40 + 85             | 64S114J                 |                         |                     |
| -55 +125             | 54S114J                 |                         |                     |

## 1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

2. Limiting conditions of use (not for inspection purposes)

|       |                                                                  |                      |      |      |             |     |                |
|-------|------------------------------------------------------------------|----------------------|------|------|-------------|-----|----------------|
| 2.1   | Minimum and maximum continuous supply voltage                    | $V_{CC}$             |      |      |             |     | -0,5V<br>+7,0V |
| 2.2   | Minimum and maximum input voltages                               |                      |      |      |             |     |                |
| 2.2.1 | Minimum and maximum input voltage                                | $V_I$                |      |      |             |     | -0,5V<br>+5,5V |
| 2.2.2 | Maximum input voltage between multiple emitter transistor inputs | $V_{II}$             |      |      |             |     | +5,5V          |
|       |                                                                  |                      |      | 54S  | 64S         | 74S | 84S            |
| 2.3   | Minimum and maximum operating ambient temperatures               | $T_{amb}(^{\circ}C)$ | min. | -55  | -40         | 0   | -25            |
|       |                                                                  |                      | max. | +125 | +85         | +70 | +85            |
| 2.4   | Minimum and maximum storage temperatures                         | $T_{stg}(^{\circ}C)$ | min. | -65  | (All types) |     |                |
|       |                                                                  |                      | max. | +150 |             |     |                |

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

| Description                                                 | Symbol    | Type             | Value                    | Unit   |
|-------------------------------------------------------------|-----------|------------------|--------------------------|--------|
| Positive supply voltage range                               | $V_{CC}$  | 54S<br>64/74/84S | 4,5 - 5,5<br>4,75 - 5,25 | V<br>V |
| Minimum value of High level input voltage                   | $V_{IHB}$ | All types        | 2,0                      | V      |
| Maximum value of High level input voltage                   | $V_{IHA}$ | All types        | 5,5                      | V      |
| Minimum value of Low level input voltage                    | $V_{ILB}$ | All types        | 0                        | V      |
| Maximum value of Low level input voltage                    | $V_{ILA}$ | All types        | 0,8                      | V      |
| Maximum value of Low level output current for each output   | $I_{OLA}$ | All types        | 20,0                     | mA     |
| Maximum value of output current for each output at $V_{OH}$ | $I_{OHA}$ | All types        | -1,0                     | mA     |
| D.C. noise margin                                           |           |                  |                          |        |
| at Low level ( $V_{ILA} - V_{OLA}$ )                        | $V_{NL}$  | All types        | 0,3                      | V      |
| at High level ( $V_{OHB} - V_{IHB}$ )                       | $V_{NH}$  | 54S<br>64/74/84S | 0,5<br>0,7               | V<br>V |

## 3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (\*)

|                       | 54S  | 64S  | 74S | 84S |    |
|-----------------------|------|------|-----|-----|----|
| T <sub>amb</sub> min. | -55  | -40  | 0   | -25 | °C |
| T <sub>amb</sub> max. | +125 | +85  | +70 | +85 |    |
| V <sub>CC</sub> min.  | 4,5  | 4,75 |     |     | V  |
| V <sub>CC</sub> max.  | 5,5  | 5,25 |     |     |    |

| Characteristics                                                      | Conditions                                                            | $V_{CC}(V)$           | Symbol      | Min. | Max.  | Unit    |
|----------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------------|-------------|------|-------|---------|
| Average supply current                                               | Q and $\bar{Q}$ outputs<br>High in turn                               | $V_{CC} \text{ max.}$ | $I_{CC}$    | -    | 50,0  | mA      |
| High level input current<br>J or K inputs<br>Clear/Clock<br>Preset   | $V_{IH(1)} = 5,5V$                                                    | $V_{CC} \text{ max.}$ | $I_{IH(1)}$ | -    | 1,0   | mA      |
|                                                                      | $V_{IH(2)} = 2,7V$                                                    | $V_{CC} \text{ max.}$ | $I_{IH(2)}$ | -    | 50,0  | $\mu A$ |
|                                                                      |                                                                       |                       | $I_{IH(2)}$ | -    | 200,0 | $\mu A$ |
|                                                                      |                                                                       |                       | $I_{IH(2)}$ | -    | 100,0 | $\mu A$ |
| Low level input current<br>J or K inputs<br>Clear<br>Preset<br>Clock | $V_{IN} = 0,5V$                                                       | $V_{CC} \text{ max.}$ | $-I_{IL}$   | -    | 1,6   | mA      |
|                                                                      |                                                                       |                       | $-I_{IL}$   | -    | 14,0  | mA      |
|                                                                      |                                                                       |                       | $-I_{IL}$   | -    | 7,0   | mA      |
|                                                                      |                                                                       |                       | $-I_{IL}$   | -    | 8,0   | mA      |
| Input clamping voltage                                               | $-I_{IC} = 18,0mA$                                                    | $V_{CC} \text{ min.}$ | $-V_{IC}$   | -    | 1,2   | V       |
| Output voltage<br>54S<br>64/74/84S<br>All types                      | $I_{OH} = -1,0mA$<br>$I_{OH} = -1,0mA$<br>$I_{OL} = 20,0mA \quad (1)$ | $V_{CC} \text{ min.}$ | $V_{OH}$    | 2,5  | -     | V       |
|                                                                      |                                                                       |                       | $V_{OH}$    | 2,7  | -     | V       |
|                                                                      |                                                                       |                       | $V_{OL}$    | -    | 0,5   | V       |

(1) Fan out = 10

| Characteristics                                                                  | Conditions                                                                           | $V_{CC}(V)$           | Symbol       | Min.          | Max.  | Unit |
|----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|-----------------------|--------------|---------------|-------|------|
| Output short circuit current                                                     | $V_{IN}$ as defined by the truth table to give High level output<br>$V_O = 0V^{(2)}$ | $V_{CC \text{ max.}}$ | $-I_{OS}$    | 40,0          | 100,0 | mA   |
| Propagation times<br>All types                                                   | $T_{amb} = 25^\circ C^*$<br>test conditions as in Sub-group A5                       | 5,0V                  |              |               |       |      |
| High to Low level<br>To From<br>Preset or Clear $\bar{Q}$ or $Q$<br>(Clock High) |                                                                                      |                       | $t_{PHL}$    | -             | 7,0   | ns   |
| Preset or Clock $\bar{Q}$ or $Q$<br>(Clock Low)                                  |                                                                                      |                       | $t_{PHL}$    | -             | 7,0   | ns   |
| Clock $Q$ or $\bar{Q}$                                                           |                                                                                      |                       | $t_{PHL}$    | -             | 7,0   | ns   |
| Low to High level<br>To From<br>Preset or Clear $Q$ or $\bar{Q}$                 |                                                                                      |                       | $t_{PLH}$    | -             | 7,0   | ns   |
| Clock $Q$ or $\bar{Q}$                                                           |                                                                                      |                       | $t_{PLH}$    | -             | 7,0   | ns   |
| Maximum clock frequency                                                          |                                                                                      |                       | $f_{clock}$  | 80,0          | -     | MHz  |
| Pulse width<br>Clock High                                                        |                                                                                      |                       | $t_w$        | 6,0           | -     | ns   |
| Clock Low                                                                        |                                                                                      |                       | $t_w$        | 6,5           | -     | ns   |
| Clear or Preset Low                                                              |                                                                                      |                       | $t_w$        | 8,0           | -     | ns   |
| Input set-up time<br>High level data                                             |                                                                                      |                       | $t_{set-up}$ | 3,0 $\dagger$ | -     | ns   |
| Low level data                                                                   |                                                                                      |                       | $t_{set-up}$ | 3,0 $\dagger$ | -     | ns   |
| Hold time                                                                        |                                                                                      |                       | $t_{hold}$   | 0 $\dagger$   | -     | ns   |

(2) Only one output at a time, duration  $t \leq 1$  sec

\*See Clause 3.1 and 3.2.1 of this specification

 $\dagger$ W.R.T falling edge of clock pulse