

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

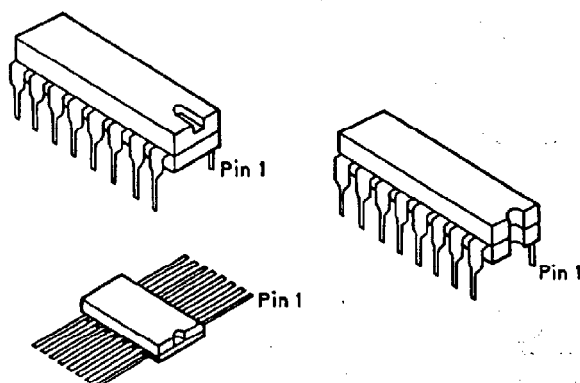
BS CECC 90102 - 028

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**ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:**BS CECC 90 000 : 1976
BS CECC 90 100 : 1977**MANUFACTURERS TYPE NUMBER**54S163
64S163
74S163
84S163Outline not to scale: Isometric projection
Marking information see clause 1Refer to IEC 191-1-50a (type A50C)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1**FULLY SYNCHRONOUS 4-BIT
BINARY COUNTERS**TYPICAL CONSTRUCTION
SILICON MONOLITHIC BIPOLAR
CAVITY AND NON-CAVITY
PACKAGES**ASSESSMENT LEVELS**
R, S, T, AND V1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

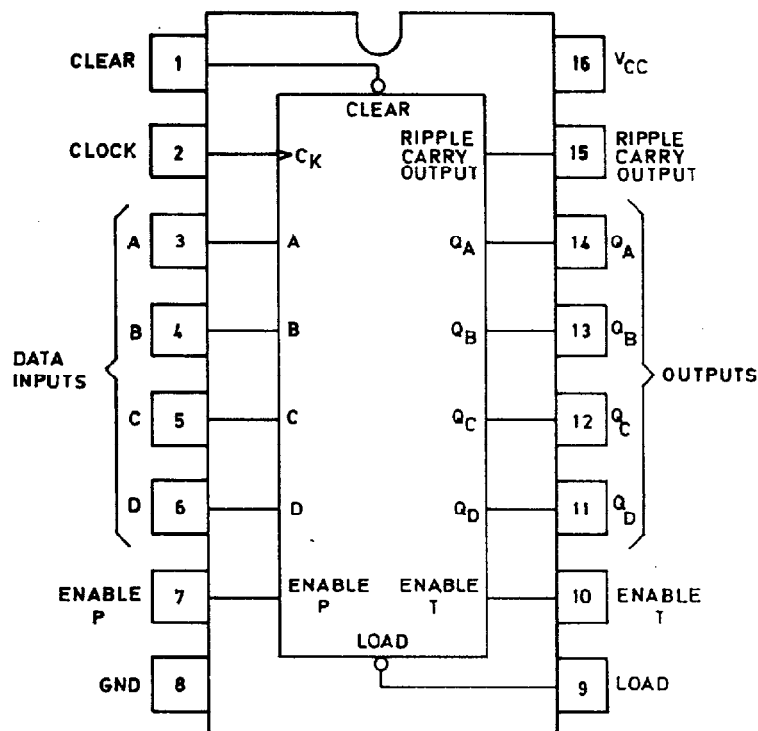
1.1 Truth table (contd)

INPUTS									OUTPUTS				
D	C	B	A	LOAD	CLEAR	ENABLE P T		CLOCK	Q _D	Q _C	Q _B	Q _A	RIPPLE CARRY
d	c	b	a	L	H	H	H	↑	d	c	b	a	X
X	X	X	X	X	X	X	X	X	H	H	H	H	H
X	X	X	X	X	L	X	X	↑	L	L	L	L	L
X	X	X	X	X	H	H	H	↑	COUNT				X
X	X	X	X	X	H	L	X	↑	INHIBIT				X
X	X	X	X	X	H	X	L	↑	INHIBIT				X

H = High level
 L = Low level
 X = Logic level irrelevant
 a,b,c,d = The respective levels of inputs A,B,C,D
 ↑ = Positive going clock transition

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Fully synchronous 4-bit counters

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S163J	N	W
-25 + 85	84S163J		
-40 + 85	64S163J		
-55 +125	54S163J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

- | | | | |
|-------|--|----------|----------------|
| 2.1 | Minimum and maximum continuous supply voltage | V_{CC} | -0,5V
+7,0V |
| 2.2 | Minimum and maximum input voltages | | |
| 2.2.1 | Minimum and maximum input voltage | V_I | -0,5V
+5,5V |
| 2.2.2 | Maximum input voltage between multiple emitter transistor inputs | V_{II} | +5,5V |

54S 64S 74S 84S

2.3 Minimum and maximum operating ambient temperatures $T_{amb}(^{\circ}C)$ min. -55 -40 0 -25
max. +125 +85 +70 +85

2.4 Minimum and maximum storage temperatures $T_{stg}(^{\circ}C)$ min. -65 (All types)
max. +150

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	0	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Maximum value of Low level output current for each output	I_{OLA}	All types	20,0	mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	All types	1,0	mA
D.C. noise margin at Low level $(V_{ILA} - V_{OLA})$	V_{NL}	All types	0,3	V
at High level $(V_{OHB} - V_{IHB})$	V_{NH}	54S 64/74/84S	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5.25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	All outputs open circuit	V_{CC} max.	I_{CC}	-	160,0	mA
High level input current	$V_{IH(1)} = 5,5V$ $V_{IH(2)} = 2,7V$	V_{CC} max. V_{CC} max.	$I_{IH(1)}$ $I_{IH(2)}$ $I_{IH(2)}$	- -10,0 -	1,0 -200,0 50,0	mA μA μA
Low level input current	$V_{IN} = 0,5V$	V_{CC} max.	$-I_{IL}$ $-I_{IL}$	- -	4,0 2,0	mA mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{IC}$	-	1,2	V
Output voltage	54S 64/74/84S All types	V_{CC} min.	V_{OH} V_{OH} V_{OL}	2,5 2,7 -	- - 0,5	V V V

(1) Fan out = 10

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output short circuit current	V_{IN} as defined by truth table to give High level output $V_O = 0V$ (2)	V_{CC} max.	$-I_{OS}$	40,0	100,0	mA
Propagation times All types	$T_{amb} = 25^{\circ}C$ * test conditions as in Sub-group A5	5,0V				
High to Low level						
From To						
Clock Ripple carry			t_{PHL}	-	25,0	ns
Clock Any Q			t_{PHL}	-	15,0	ns
Enable T Ripple carry			t_{PHL}	-	15,0	ns
Low to High level						
From To						
Clock Ripple carry			t_{PLH}	-	25,0	ns
Enable T Ripple carry			t_{PLH}	-	15,0	ns
Clock Any Q			t_{PLH}	-	15,0	ns
Maximum clock frequency			$f_{(clock)}$	40,0	-	MHz
Duration of clock pulse			$t_{p(clock)}$	10,0	-	ns
Duration of clear pulse			$t_{p(clear)}$	10,0	-	ns
Set-up time						
Load or Clear input			$t_{(set-up)}$	14,0	-	ns
Enable P or T inputs			$t_{(set-up)}$	12,0	-	ns
Data inputs A,B,C,D			$t_{(set-up)}$	4,0	-	ns
Data hold time						
Data inputs A,B,C,D			$t_{(hold)}$	3,0	-	ns
Load and Clear inputs			$t_{(hold)}$	0	-	ns

(2) Only one output at a time, duration $t \leq 1$ sec

*See Clauses 3.1 and 3.2.1 of this specification