



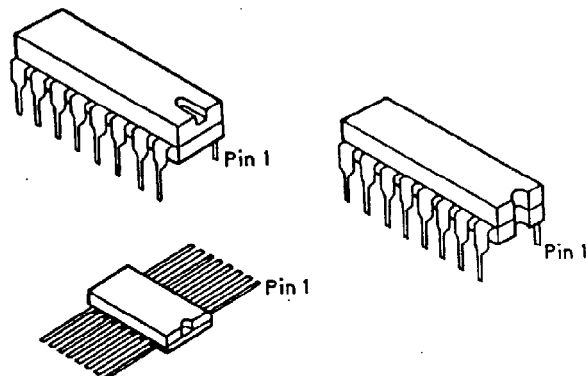
**ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:**

BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54S169
64S169
74S169
84S169

Outline not to scale: Isometric projection
Marking information see clause 1



Refer to IEC 191-1-50a (type A50C)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)

SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1

**4-BIT UP/DOWN SYNCHRONOUS
BINARY COUNTER**

TYPICAL CONSTRUCTION
SILICON MONOLITHIC BIPOLAR
CAVITY AND NON-CAVITY
PACKAGES

ASSESSMENT LEVELS
R, S, T, AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

	U/ $\overline{D}$	CLOCK	A B C D	ENABLE $\overline{P}$	ENABLE $\overline{T}$	LOAD	OUTPUT				RIPPLE CARRY
							Q_A	Q_B	Q_C	Q_D	
Load	X	$\uparrow$	A B C D	X	X	$\overline{L}$	Q_A	Q_B	Q_C	Q_D	$\$$
Count-up	H	$\uparrow$	X X X X	L	L	H	Q_A	Q_B	Q_C	Q_D	
	H	$\uparrow$	X X X X	L	L	H	Q_{AN}	Q_{BN}	Q_{CN}	Q_{DN}	
e.g. 13	H	$\uparrow$	X X X X	L	L	H	H	L	H	H	H
to 14	H	$\uparrow$	X X X X	L	L	H	L	H	H	H	H
to 15	H	$\uparrow$	X X X X	L	L	H	H	H	H	H	L
to 0	H	$\uparrow$	X X X X	L	L	H	L	L	L	L	H
Inhibit	X	X	X X X X	H	H	H	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	Q_{RO}
Count-down	L	$\uparrow$	X X X X	L	L	H	Q_A	Q_B	Q_C	Q_D	Q_R
	L	$\uparrow$	X X X X	L	L	H	Q_{AN-1}	Q_{BN-1}	Q_{CN-1}	Q_{DN-1}	Q_{RN-1}

H = High logic level

L = Low logic level

 $\$$ = Ripple carry output = H until count reaches maximum or minimum value

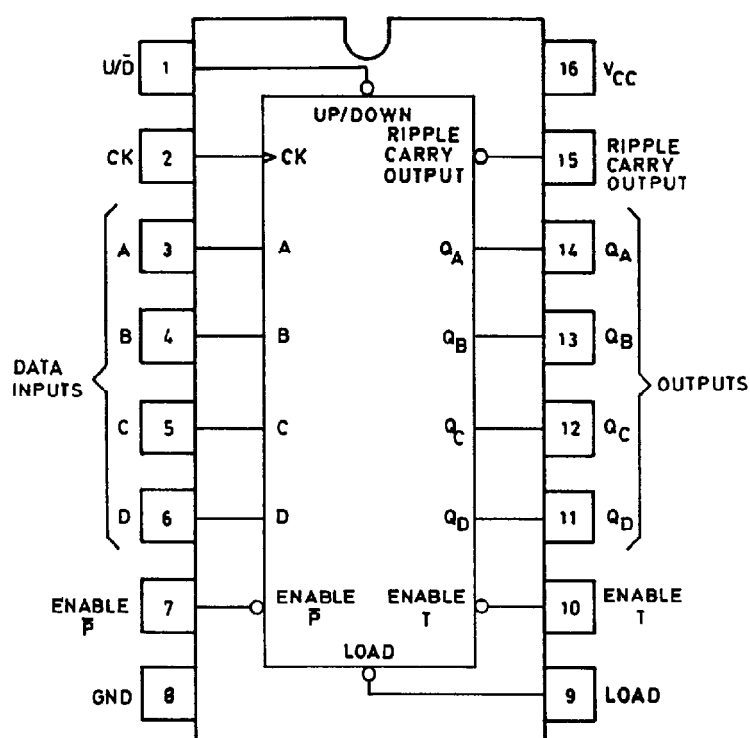
 $\uparrow$ = Positive clock transition

 $\overline{L}$ = Negative pulse from High logic level

 Q_A, Q_B, Q_C, Q_D = Output conditions at 1st pulse of load

 $Q_{AN}, Q_{BN}, Q_{CN}, Q_{DN}$ = Output conditions 1 count increase after Q_A
 $Q_{AN-1}, Q_{BN-1}, Q_{CN-1}, Q_{DN-1}$ = Output conditions 1 count decrease after Q_A

1.2.1 Terminal identification



4-bit up/down synchronous binary counter

This synchronous presettable counter features an internal carry look-ahead for cascading in high-speed counting applications. The S169 is a Binary Counter. Synchronous operation is provided by having all bistables clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave bistables on the rising (positive-going) edge of the clock waveform.

This counter is fully programmable; that is the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\bar{P}$ and $\bar{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\bar{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the lower portion of Q_A output when counting down. This low-level overflow carry pulse

can be used to enable successive cascaded stages. Transitions at the enable $\bar{P}$ or $\bar{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimise transition-line effects, thereby simplifying system design.

This counter features a fully independent clock circuit. Changes at control inputs (enable $\bar{P}$, enable $\bar{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S169J	N	W
-25 + 85	84S169J		
-40 + 85	64S169J		
-55 +125	54S169J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2.	<u>Limiting conditions of use</u> (not for inspection purposes)				■ 1974499 0006747 T66 ■
2.1	Minimum and maximum continuous supply voltage	V_{CC}			-0,5V +7,0V
2.2	Minimum and maximum input voltages				
2.2.1	Minimum and maximum input voltage	V_I			-0,5V +5,5V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}			+5,5V
			54S	64S	74S 84S
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	-55	-40 0 -25
			max.	+125	+85 +70 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)
			max.	+150	

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	0	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Maximum value of Low level output current for each output	I_{OLA}	All types	20,0	mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	All types	1,0	mA
D.C. noise margin				
at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54S 64/74/84S	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(\text{V})$	Symbol	Min.	Max.	Unit
Total supply current per package	Clock input = momentary 4,5V then 0V. All other inputs = 0V. All outputs open.	$V_{CC} \text{ max.}$	I_{CC}	-	160,0	mA
High level input current Load Enable $\bar{T}$ Other inputs	$V_{IH(1)} = 5,5\text{V}$ $V_{IH(2)} = 2,7\text{V}$	$V_{CC} \text{ max.}$	$I_{IH(1)}$ $I_{IH(2)}$ $I_{IH(2)}$ $I_{IH(2)}$	- 10,0 - -	1,0 -200,0 100,0 50,0	mA μA μA μA
Low level input current Enable $\bar{T}$ Other outputs	$V_{IN} = 0,5\text{V}$	$V_{CC} \text{ max.}$	$-I_{IL}$ $-I_{IL}$	- -	4,0 2,0	mA mA
Input clamping voltage	$-I_{IC} = 18,0\text{mA}$	$V_{CC} \text{ min.}$	$-V_{IC}$	-	1,2	V
Output voltage 54S 64/74/84S All types	$-I_{OH} = 1,0\text{mA}$ $-I_{OH} = 1,0\text{mA}$ $I_{OL} = 20,0\text{mA} \quad (1)$	$V_{CC} \text{ min.}$	V_{OH} V_{OH} V_{OL}	2,5 2,7 -	- - 0,5	V V V
Output short circuit current	V_{IN} as defined by truth table to give High level output $V_O = 0\text{V} \quad (2)$	$V_{CC} \text{ max.}$	$-I_{OS}$	40,0	100,0	mA

(1) Fan out = 10 (2) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See clauses 3.1 and 3.2.1 of this specification

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Propagation times All types	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
High to Low level						
From To						
Clock Ripple carry			t_{PHL}	-	28,0	ns
Clock Any Q			t_{PHL}	-	15,0	ns
Enable $\bar{T}$ Ripple carry			t_{PHL}	-	22,0	ns
Up/Down Ripple carry			t_{PHL}	-	15,0	ns
Low to High level						
From To						
Clock Ripple carry			t_{PLH}	-	21,0	ns
Clock Any Q			t_{PLH}	-	15,0	ns
Enable $\bar{T}$ Ripple carry			t_{PLH}	-	11,0	ns
Up/Down Ripple carry			t_{PLH}	-	15,0	ns
Maximum clock frequency			f_{clock}	-	40,0	MHz
Width of clock pulse			$t_{p(clock)}$	10,0	-	ns
Hold time at any input w.r.t clock			$t_{(hold)}$	1,0	-	ns
Set-up time Data inputs A, B, C, D			$t_{(set-up)}$	4,0	-	ns
Enable $\bar{P}$ or $\bar{T}$			$t_{(set-up)}$	14,0	-	ns
Load			$t_{(set-up)}$	6,0	-	ns
Up/Down			$t_{(set-up)}$	20,0	-	ns

*See clauses 3.1 and 3.2.1 of this specification