

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90102 - 033

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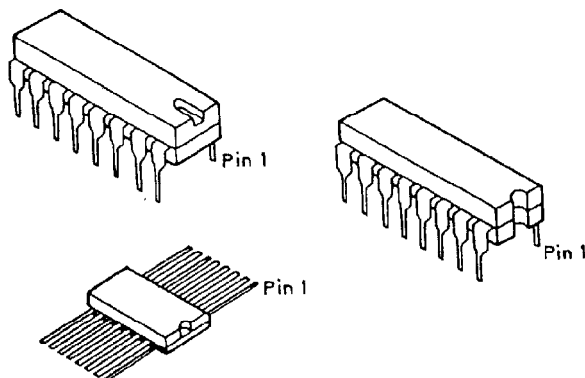
ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:

BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54S194
64S194
74S194
84S194

Outline not to scale: Isometric projection
Marking information see clause 1



Refer to IEC 191-1-50a (type A50C)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)

SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1

4-BIT BI-DIRECTIONAL
UNIVERSAL SHIFT REGISTERS

TYPICAL CONSTRUCTION
SILICON MONOLITHIC BIPOLAR
CAVITY AND NON-CAVITY
PACKAGES

ASSESSMENT LEVELS
R, S, T, AND V

1. Type description

1.1 Truth table (see page 2)

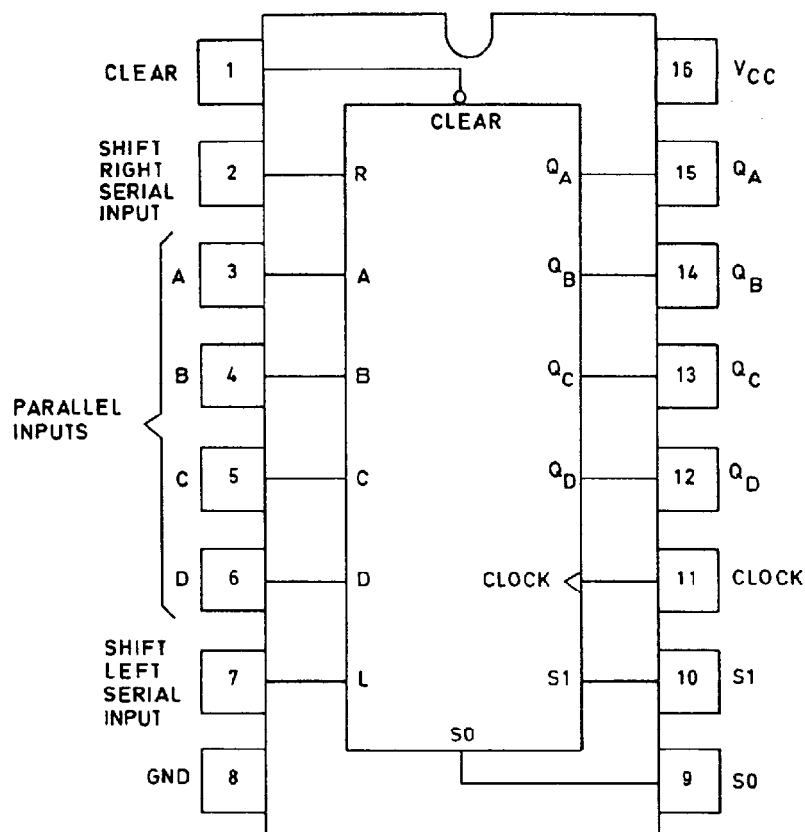
Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D
	S ₁	S ₀		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}
H	H	L	↑	H	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}

- H = High level (steady level)
 L = Low level (steady level)
 X = Logic level irrelevant (any input, including transitions)
 ↑ = Transition from Low to High level
 a,b,c,d = The level of steady-level input at inputs A,B,C, or D respectively
 Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO} = The level of Q_A, Q_B, Q_C or Q_D respectively, before the indicated steady level input conditions were established
 Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, Q_D respectively, before the most recent ↑ transition of the clock

1.2 Terminal identification, type designation and marking



4-bit bi-directional universal shift registers

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S194AJ	N	W
-25 + 85	84S194AJ		
-40 + 85	64S194AJ		
-55 +125	54S194AJ		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Minimum and maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Minimum and maximum input voltages							
2.2.1	Minimum and maximum input voltage	V_I						-0,5V +5,5V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
				54S	64S	74S	84S	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

3.1 (contd)

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	0	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Maximum value of Low level output current for each output	I_{OLA}	All types	20,0	mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-1,0	mA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54S 64/74/84S	0,3 0,5 0,7	V V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	Inputs and outputs open circuit	V_{CC} max.	I_{CC}	-	135,0	mA
High level input current	$V_{IH(1)} = 5,5V$ $V_{IH(2)} = 2,4V$	V_{CC} max.	$I_{IH(1)}$	-	1,0	mA
		V_{CC} max.	$I_{IH(2)}$	-	50,0	μA
Low level input current	$V_{IN} = 0,5V$	V_{CC} max.	$-I_{IL}$	-	2,0	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{IC}$	-	1,2	V
Output voltage 54S 64/74/84S All types	$-I_{OH} = 1,0mA$ $-I_{OH} = 1,0mA$ $I_{OL} = 20,0mA$ (1)	V_{CC} min.	V_{OH}	2,5	-	V
			V_{OH}	2,7	-	V
			V_{OL}	-	0,5	V
Output short circuit current	V_{IN} as defined by truth table to give High level output $V_O = 0V$ (2)	V_{CC} max.	$-I_{OS}$	40,0	100,0	mA
Propagation times All types	$T_{amb} = 25^{\circ}C^*$ conditions as in Sub-group A5	5,0V				
High to Low level Output from Clear			t_{PHL}	-	18,5	ns
Output from Clock			t_{PHL}	-	16,5	ns
Low to High level Output from Clock			t_{PLH}	-	12,0	ns
Maximum clock frequency			$f_{(max)}$	70,0	-	MHz
Width of clock pulse			$t_{p(clock)}$	7,0	-	ns
Width of clear pulse			$t_{p(clear)}$	12,0	-	ns

(1) Fan out = 10

(2) Only one output at a time, duration $t \leq 1$ sec

*See clauses 3.1 and 3.2.1 of this specification