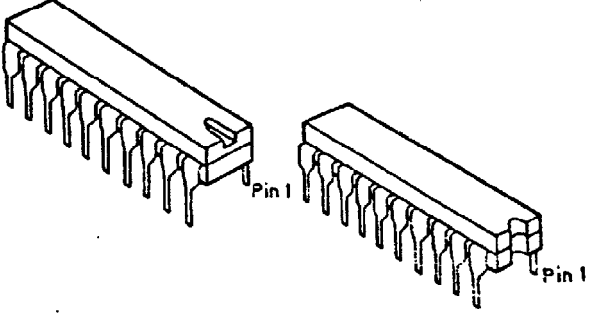


|                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                           |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>BRITISH STANDARDS INSTITUTION</b><br>2 PARK STREET, LONDON. W1A 2BS                                                                                                                                                           | BS CECC 90102 - 035<br><br>ISSUE 1<br><br>JANUARY 1982<br><br>Page 1 of 19 pages                                                                                                                                                                          |
| Specification available from:- AS SHOWN IN PD 9002<br>AND CECC 00 200 AND                                                                                                                                                        |                                                                                                                                                                        |
| <b>ELECTRONIC COMPONENTS OF ASSESSED QUALITY</b><br><b>DETAIL SPECIFICATION IN ACCORDANCE WITH:</b><br><br>BS CECC 90 000 : 1976<br>BS CECC 90 100 : 1977                                                                        | <b>MANUFACTURERS TYPE NUMBER</b><br><br>54S241<br>64S241<br>74S241<br>84S241<br><br>SEE PD 9002 AND CECC 00 200<br>For ordering information see<br>clause 1                                                                                               |
| Outline not to scale: Isometric projection<br>Marking information see clause 1<br><br><br><br>refer to Appendix A1.3<br>Dual-in-Line (ceramic) | <b>OCTAL BUFFER AND LINE-DRIVER WITH COMPLEMENTARY G AND <math>\bar{G}</math> INPUTS AND THREE LEVEL OUTPUT</b><br><br>TYPICAL CONSTRUCTION<br>SILICON MONOLITHIC BIPOLAR<br>CAVITY AND NON-CAVITY<br>PACKAGES<br><br>ASSESSMENT LEVELS<br>R, S, T, AND V |

1. Type description

## 1. Truth table (each gate)

| INPUTS    |    | OUTPUTS |
|-----------|----|---------|
| $\bar{G}$ | 1A | Y       |
| H         | X  | Z       |
| L         | H  | H       |
| L         | L  | L       |

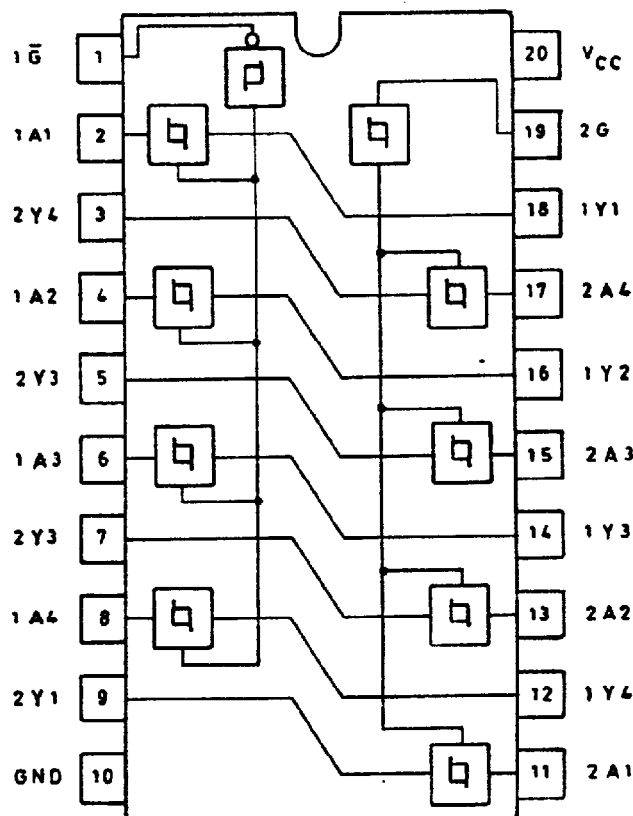
| INPUTS |    | OUTPUTS |
|--------|----|---------|
| G      | 2A | Y       |
| L      | X  | Z       |
| H      | H  | H       |
| H      | L  | L       |

H = High level  
 L = Low level  
 X = Logic level irrelevant  
 Z = High impedance

Refer to Qualified Products List PD 9002 and/or CECC 00 200 for details of manufacturers approved to this specification

## 1.2 Terminal identification, type designation and marking

## 1.2.1 Terminal identification



Octal buffer and line driver with three level output

## Three level device

A device whose output can be driven into a High, Low or high impedance level

## High impedance level

That level of a device in which the output acquires a high impedance characteristic

## High impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high impedance level

## 1.2.2 Type designation

| TEMPERATURE<br>RANGE | PACKAGE                 |                         |                     |
|----------------------|-------------------------|-------------------------|---------------------|
|                      | Ceramic<br>Dual-in-Line | Plastic<br>Dual-in-Line | Ceramic<br>Flatpack |
| 0 + 70               | 74S241J                 | N                       | W                   |
| -25 + 85             | 84S241J                 |                         |                     |
| -40 + 85             | 64S241J                 |                         |                     |
| -55 +125             | 54S241J                 |                         |                     |

## 1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

## 1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

|                                                                        |                      |              |             |             |          |            |
|------------------------------------------------------------------------|----------------------|--------------|-------------|-------------|----------|------------|
| Minimum and maximum continuous supply voltage                          | $V_{CC}$             |              | -0,5V       | +7,0V       |          |            |
| 2.2 Minimum and maximum input voltages                                 |                      |              |             |             |          |            |
| 2.2.1 Minimum and maximum input voltages                               | $V_I$                |              | -0,5V       | +5,5V       |          |            |
| 2.2.2 Maximum input voltage between multiple emitter transistor inputs | $V_{II}$             |              | +5,5V       |             |          |            |
| 2.3 Minimum and maximum operating ambient temperatures                 | $T_{amb}(^{\circ}C)$ | min.<br>max. | -55<br>+125 | -40<br>+85  | 0<br>+70 | -25<br>+85 |
| 2.4 Minimum and maximum storage temperatures                           | $T_{stg}(^{\circ}C)$ | min.<br>max. | -65<br>+150 | (All types) |          |            |

### 3. Recommended operating conditions and associated characteristics (not for inspection purposes)

#### 3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

| Description                                                                                        | Symbol                  | Type                          | Value                    | Unit               |
|----------------------------------------------------------------------------------------------------|-------------------------|-------------------------------|--------------------------|--------------------|
| Positive supply voltage range                                                                      | $V_{CC}$                | 54S<br>64/74/84S              | 4,5 - 5,5<br>4,75 - 5,25 | V<br>V             |
| Minimum value of High level input voltage                                                          | $V_{IHB}$               | All types                     | 2,0                      | V                  |
| Maximum value of High level input voltage                                                          | $V_{IHA}$               | All types                     | 5,5                      | V                  |
| Minimum value of Low level input voltage                                                           | $V_{ILB}$               | All types                     | -0,3                     | V                  |
| Maximum value of Low level input voltage                                                           | $V_{ILA}$               | All types                     | 0,8                      | V                  |
| Maximum value of Low level output current for each output                                          | $I_{OLA}$               | 54S<br>64/74/84S              | 48,0<br>64,0             | mA<br>mA           |
| Maximum value of output current for each output at $V_{OH}$                                        | $-I_{OHA}$              | 54S<br>64/74/84S              | 12,0<br>15,0             | mA<br>mA           |
| High impedance level output current (leakage)<br>$V_{OUT} = 2,4V$<br>$V_{OUT} = 0,5V$              | $I_{OHZ}$<br>$-I_{OLZ}$ | All types<br>All types        | 50,0<br>50,0             | $\mu A$<br>$\mu A$ |
| D.C. noise margin<br>at Low level ( $V_{ILA} - V_{OLA}$ )<br>at High level ( $V_{OHB} - V_{IHB}$ ) | $V_{NL}$<br>$V_{NH}$    | All types<br>54S<br>64/74/84S | 0,3<br>0,5<br>0,7        | V<br>V<br>V        |

#### 3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (\*)

## 3.2.1 (contd)

|                       | 54S  | 64S  | 74S | 84S |    |
|-----------------------|------|------|-----|-----|----|
| T <sub>amb</sub> min. | -55  | -40  | 0   | -25 | °C |
| T <sub>amb</sub> max. | +125 | +85  | +70 | +85 |    |
| V <sub>CC</sub> min.  | 4,5  | 4,75 |     |     | V  |
| V <sub>CC</sub> max.  | 5,5  | 5,25 |     |     |    |

## 3.2.2

| Characteristics          | Conditions                          | $V_{CC}(V)$   | Symbol      | Min. | Max.  | Unit    |
|--------------------------|-------------------------------------|---------------|-------------|------|-------|---------|
| Total supply current     | 54S Outputs High                    | $V_{CC}$ max. | $I_{CC}$    | -    | 147,0 | mA      |
|                          | 64/74/84S Outputs High              |               | $I_{CC}$    | -    | 160,0 | mA      |
|                          | 54S Outputs open                    |               | $I_{CC}$    | -    | 170,0 | mA      |
|                          | 64/74/84S Outputs Low               |               |             | -    | 180,0 | mA      |
|                          | 54S Outputs open                    |               | $I_{CC}$    | -    | 170,0 | mA      |
|                          | 64/74/84S Outputs disabled          |               |             | -    | 180,0 | mA      |
|                          | Outputs open                        |               | $I_{CC}$    | -    | 180,0 | mA      |
| High level input current | $V_{IH(1)} = 5,5V$                  | $V_{CC}$ max. | $I_{IH(1)}$ | -    | 1,0   | mA      |
|                          | $V_{IH(2)} = 2,7V$                  | $V_{CC}$ max. | $I_{IH(2)}$ | -    | 50,0  | $\mu A$ |
| Low level input current  | $V_{IN} = 0,5V$                     | $V_{CC}$ max. | $-I_{IL}$   | -    | 400,0 | $\mu A$ |
|                          |                                     |               | $-I_{IL}$   | -    | 2,0   | mA      |
| Input clamping voltage   | $-I_{IC} = 18,0mA$                  | 5,0V          | $-V_{IC}$   | -    | 1,2   | V       |
| Output voltage           | 54S $-I_{OUT} = 3,0mA$              | $V_{CC}$ min. | $V_{OH}$    | 2,4  | -     | V       |
|                          | 64/74/84S $-I_{OUT} = I_{OHA}^*$    |               | $V_{OH}$    | 2,0  | -     | V       |
|                          | All types $I_{OUT} = I_{OLA}^* (1)$ |               | $V_{OL}$    | -    | 0,5   | V       |

(1) Fan out = 24(54S)  
= 32 (64/74/84S)

\*See 3.2.1 of this specification

## 3.2.2 (contd)

| Characteristics                        | Conditions                                                       | $V_{CC}(V)$           | Symbol    | Min. | Max.  | Unit |
|----------------------------------------|------------------------------------------------------------------|-----------------------|-----------|------|-------|------|
| Output short circuit current           | $V_{IN} = 0V$ (2)<br>$V_O = 0V$ (3)                              | $V_{CC} \text{ max.}$ | $-I_{OS}$ | 50,0 | 225,0 | mA   |
| Propagation times<br>All types         | $T_{amb} = 25^{\circ}C$<br>test conditions as<br>in Sub-group A5 | 5,0V                  |           |      |       |      |
| High to Low level                      |                                                                  |                       | $t_{PHL}$ | -    | 9,0   | ns   |
| Low to High level                      |                                                                  |                       | $t_{PLH}$ | -    | 9,0   | ns   |
| Output enable time<br>to Low level     |                                                                  |                       | $t_{PZL}$ | -    | 15,0  | ns   |
| Output enable time<br>to High level    |                                                                  |                       | $t_{PZH}$ | -    | 12,0  | ns   |
| Output disable time<br>from Low level  | $C_L = 5pF$                                                      |                       | $t_{PLZ}$ | -    | 15,0  | ns   |
| Output disable time<br>from High level | $C_L = 5pF$                                                      |                       | $t_{PHZ}$ | -    | 9,0   | ns   |

(2) To all inputs

(3) Only one output at a time, duration  $t \leq 1s$ 

\*See 3.2.1 of this specification

## 3.3 Supplementary information

## 3.3.1 Change of typical propagation time with output loading

