BRITISH STANDARDS INSTITUTION
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BS CECC 90102 - 042

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Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND

ELECTRONIC COMPONENTS OF ASSESSED QUALITY

DETAIL SPECIFICATION IN ACCORDANCE WITH:

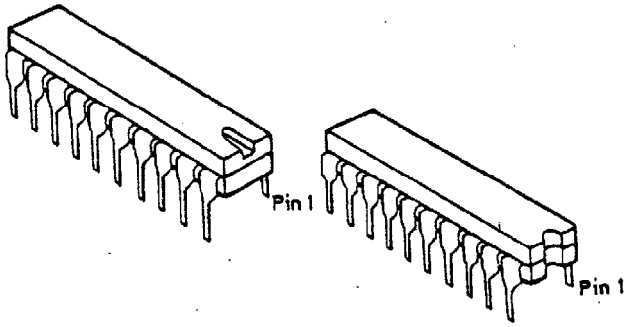
BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54S244
64S244
74S244
84S244

SEE PD 9002 AND CECC 00 200
For ordering information see clause 1

Outline not to scale: Isometric projection
Marking information see clause 1



refer to Appendix A1.3
Dual-in-Line (ceramic)

OCTAL BUFFER AND LINE-DRIVER WITH THREE LEVEL OUTPUTS

TYPICAL CONSTRUCTION
SILICON MONOLITHIC BIPOLAR
CAVITY AND NON-CAVITY PACKAGES

ASSESSMENT LEVELS
R, S, T, AND V

1. Type description

1.1 Truth table (each gate)

INPUTS		OUTPUTS
$\overline{G}$	1A	Y
H	X	Z
L	H	H
L	L	L

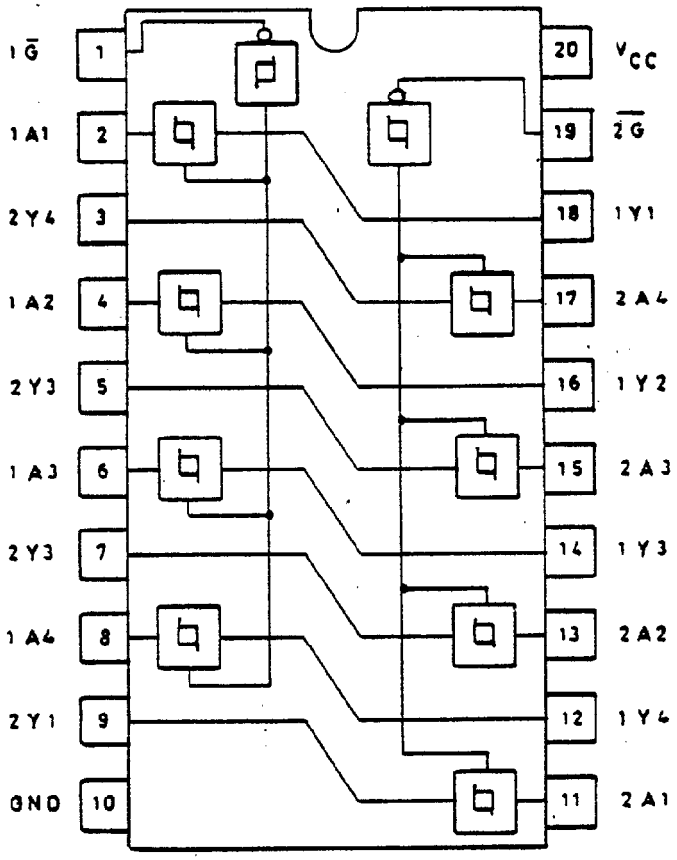
H = High level
L = Low level
X = Logic level irrelevant
Z = High impedance

Refer to Qualified Products List PD 9002 and/or CECC 00 200 for details of manufacturers approved to this specification

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1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Octal buffer and line driver with three level output

Three level device	A device whose output can be driven into a High, Low or high impedance level
High impedance level	That level of a device in which the output acquires a high impedance characteristic
High impedance leakage current	The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high impedance level

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1.2.2 Type designation

TEMPERATURE RANGE		PACKAGE	
		Ceramic Dual-in-Line	Plastic Dual-in-Line
0	+ 70	74S244J	74S244N
-25	+ 85	84S244J	
-40	+ 85	64S244J	
-55	+125	54S244J	

1.2.3 Marking

Each integrated circuit shall bear the following markings:

(1) Terminal identification
(2) Type designation
(3) Date code
(4) Factory identification code (unless derived from trademark)
(5) Manufacturers trade name or mark
(6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Minimum and maximum continuous supply voltage	V_{CC}					-0,5V +7,0V
2.2	Minimum and maximum input voltages						
2.2.1	Minimum and maximum input voltages	V_I					-0,5V +5,5V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}					+5,5V
				54S	64S	74S	84S
2.3	Minimum and maximum operating ambient temperatures	$T_{amb(^oC)}$,	min. max.	-55 +125	-40 +85	0 +70	-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg(^oC)}$	min. max.	-65 +150	(All types)		

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3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Maximum value of Low level output current for each output	I_{OLA}	54S 64/74/84S	48,0 64,0	mA mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	54S 64/74/84S	12,0 15,0	mA mA
High impedance level output current (leakage) V_{OUT} = 2,4V V_{OUT} = 0,5V	I_{OHZ} $-I_{OLZ}$	All types All types	50,0 50,0	µA µA
D.C. noise margin at Low level $(V_{ILA} - V_{OLA})$ at High level $(V_{OHB} - V_{IHB})$	V_{NL} V_{NH}	All types 54S 64/74/84S	0,3 0,5 0,7	V V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

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.2.1 (contd)

	54S	64S	74S	84S	
T_{amb} min.	-55	-40	0	-25	°C
T_{amb} max.	+125	+85	+70	+85	
V_{CC} min.	4,5	4,75			V
V_{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC(V)}$	Symbol	Min.	Max.	Unit
Total supply current		V_{CC} max.				
54S	Outputs High		I_{CC}	-	147,0	mA
64/74/84S	Outputs High		I_{CC}	-	160,0	mA
	Outputs open					
54S	Outputs Low		I_{CC}	-	170,0	mA
64/74/84S	Outputs Low		I_{CC}	-	180,0	mA
	Outputs open					
54S	Outputs disabled		I_{CC}	-	170,0	mA
64/74/84S	Outputs disabled		I_{CC}	-	180,0	mA
	Outputs open					
High level input current	$V_{IH(1)}$ = 5,5V	V_{CC} max.	$I_{IH(1)}$	-	1,0	mA
	$V_{IH(2)}$ = 2,7V	V_{CC} max.	$I_{IH(2)}$	-	50,0	µA
Low level input current	V_{IN} = 0,5V	V_{CC} max.				
Any A input			$-I_{IL}$	-	400,0	µA
Any G input			$-I_{IL}$	-	2,0	mA
Input clamping voltage	$-I_{IC}$ = 18,0mA	5,0V	$-V_{IC}$	-	1,2	V
Output voltage		V_{CC} min.				
54S	$-I_{OUT}$ = 3,0mA		V_{OH}	2,4	-	V
64/74/84S	$-I_{OUT}$ = I_{OHA}*		V_{OH}	2,0	-	V
All types	I_{OUT} = I_{OLA}* (1)		V_{OL}	-	0,5	V

(1) Fan out = 24(54S)
= 32 (64/74/84S)

*See 3.2.1 of this specification

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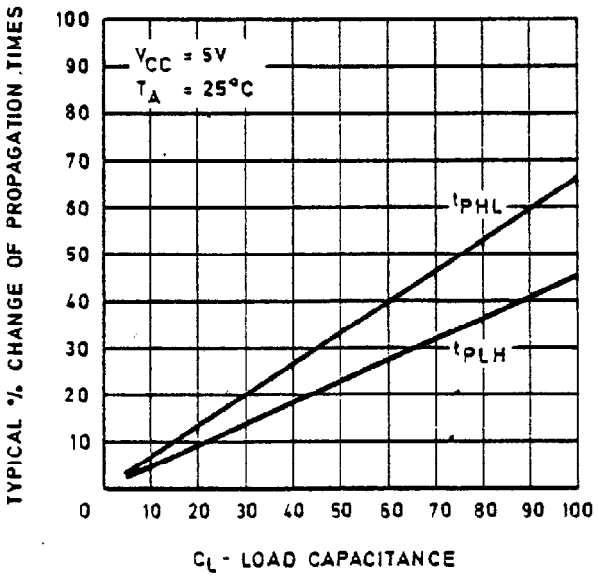
3.2.2 (contd)

Characteristics	Conditions	$V_{CC(V)}$	Symbol	Min.	Max.	Unit
Output short circuit current	V_{IN} = OV (2) V_O = OV (3)	V_{CC} max.	$-I_{OS}$	50,0	225,0	mA
Propagation times All types	T_{amb} = 25°C* test conditions as in Sub-group A5	5,0V				
High to Low level			t_{PHL}	-	9,0	ns
Low to High level			t_{PLH}	-	9,0	ns
Output enable time to Low level			t_{PZL}	-	15,0	ns
Output enable time to High level			t_{PZH}	-	12,0	ns
Output disable time from Low level	C_L = 5pF		t_{PLZ}	-	15,0	ns
Output disable time from High level	C_L = 5pF		t_{PHZ}	-	9,0	ns

(2) To all inputs
(3) Only one output at a time, duration t ≤ 1s
*See 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



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