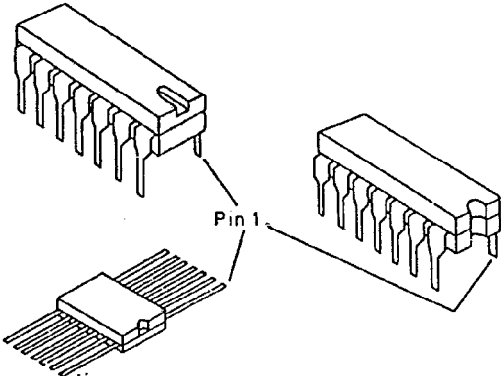


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90102 - 048 ISSUE 1 OCTOBER 1982 Page 1 of 19 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54S113 64S113 74S113 84S113 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50B) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	DUAL J-K NEGATIVE-EDGE-TRIGGERED BISTABLE CIRCUIT WITH PRESET TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR CAVITY AND NON-CAVITY PACKAGES ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200 for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	$\bar{L}$
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

H = High level

L = Low level

X = Logic level irrelevant

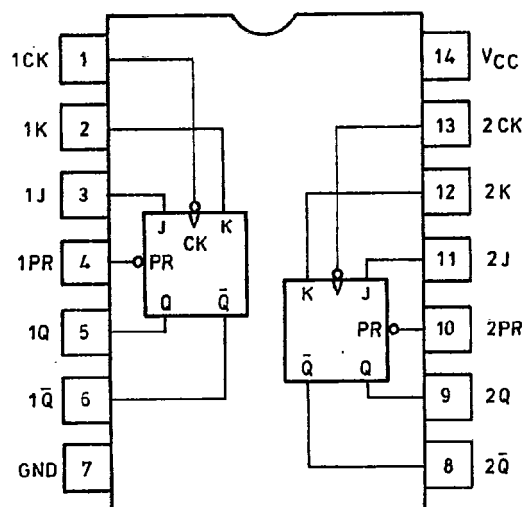
↓ = Transition from High to Low level

 Q_0 = The level of Q before the indicated input conditions were established

TOGGLE = Each output changes to the complement of its previous level on each active transition of the clock

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Dual J-K negative-edge-triggered bistable circuit with preset

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S113J	N	W
-25 + 85	84S113J		
-40 + 85	64S113J		
-55 +125	54S113J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used).

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

2. Limiting conditions of use (not for inspection purposes)

2.1	Minimum and maximum continuous supply voltage	V_{CC}	-0,5V +7,0V				
2.2	Minimum and maximum input voltages						
2.2.1	Minimum and maximum input voltage	V_I	-0,5V +5,5V				
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V				
			54S	64S	74S	84S	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85	0 +70	-25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Maximum value of Low level output current for each output	I_{OLA}	All types	20,0	mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-1,0	mA
D.C. noise margin				
at Low Level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54S 64/74/84S	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(\text{V})$	Symbol	Min.	Max.	Unit
Total supply current	Outputs open circuit 0V to Clock	V_{CC} max.	I_{CC}	-	50,0	mA
High level input current J or K inputs Clock/Preset	$V_{IH(1)} = 5,5\text{V}$ $V_{IH(2)} = 2,7\text{V}$	V_{CC} max.	$I_{IH(1)}$	-	1,0	mA
			$I_{IH(2)}$	-	50,0	μA
			$I_{IH(2)}$	-	100,0	μA
Low level input current J or K inputs Preset Clock	$V_{IN} = 0,5\text{V}$	V_{CC} max.	$-I_{IL}$	-	1,6	mA
			$-I_{IL}$	-	7,0	mA
			$-I_{IL}$	-	4,0	mA
Input clamping voltage	$-I_{IC} = 18,0\text{mA}$	V_{CC} min.	$-V_{IC}$	-	1,2	V
Output voltage 54S 64/74/84S All types	$I_{OH} = -1,0\text{mA}$ $I_{OH} = -1,0\text{mA}$ $I_{OL} = 20,0\text{mA}^{(1)}$	V_{CC} min.	V_{OH}	2,5	-	V
			V_{OH}	2,7	-	V
			V_{OL}	-	0,5	V

(1) Fan out = 10

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output short circuit current	V_{IN} as defined by the truth table to give High level output $V_O = 0V^{(2)}$	V_{CC} max.	$-I_{OS}$	40,0	100,0	mA
Propagation times All types	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
High to Low level From $\overline{Q}$ or $\overline{Q}$ Preset or Clock (as appropriate)			t_{PHL}	-	7,0	ns
Low to High level From Q or $\overline{Q}$ Preset or Clock (as appropriate)			t_{PLH}	-	7,0	ns
Maximum clock frequency			f_{clock}	80,0	-	MHz
Pulse durations Clock High Clock Low Preset Low			$t_{p(clock)}$ $t_{p(clock)}$ t_p (preset)	6,0 6,5 8,0	- - -	ns ns ns
Set-up time			t_{set-up}	3,0†	-	ns
Hold time			t_{hold}	0†	-	ns

(2) Only one output at a time, duration $t \leq 1s$

*See Caluses 3.1 and 3.2.1 of this specification

†W.R.T. falling edge of clock pulse