

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90102 - 050

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Page 1 of 19 pages

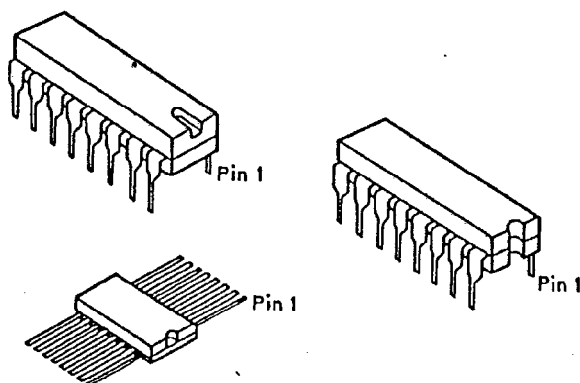
ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:

BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54S138
64S138
74S138
84S138

Outline not to scale: Isometric projection
Marking information see clause 1



Refer to IEC 191-1-50a (type A50C)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)

SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1

3-TO-8 LINE DECODERS/
DEMULPLEXERS

TYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR CAVITY AND NON-
CAVITY PACKAGES

ASSESSMENT LEVELS
R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

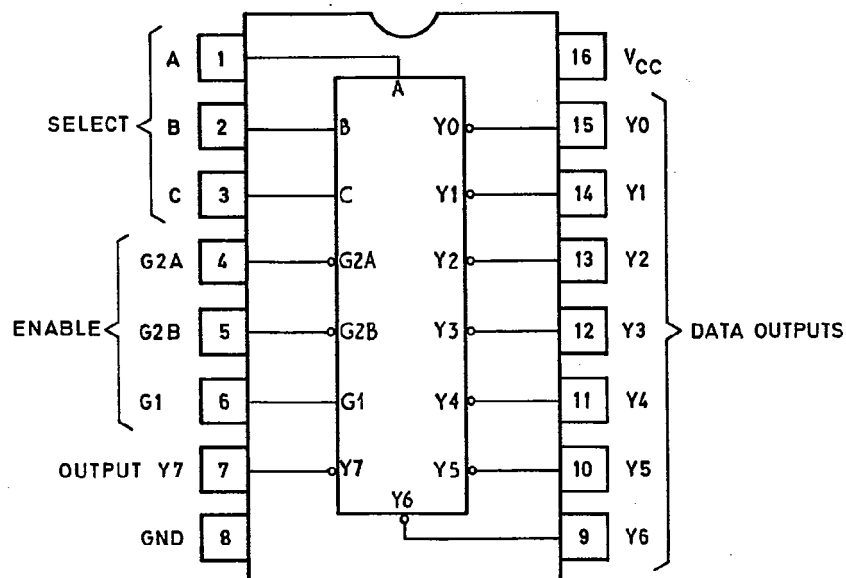
1.1 Truth tables (contd)

INPUTS					OUTPUTS								
ENABLE		SELECT											
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
X	H	X	X	X	H	H	H	H	H	H	H	H	
L	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	H	H	H	H	H	H	H	
H	L	L	L	H	H	L	H	H	H	H	H	H	
H	L	L	H	L	H	H	L	H	H	H	H	H	
H	L	L	H	H	H	H	H	L	H	H	H	H	
H	L	H	L	L	H	H	H	H	L	H	H	H	
H	L	H	L	H	H	H	H	H	H	L	H	H	
H	L	H	H	L	H	H	H	H	H	H	L	H	
H	L	H	H	H	H	H	H	H	H	H	H	L	

H = High level
 L = Low level
 X = Level irrelevant
 $G2* = G2A + G2B$

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



3-to-8 line decoders/demultiplexers

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S138J	N	W
-25 + 85	84S138J		
-40 + 85	64S138J		
-55 +125	54S138J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Minimum and maximum continuous supply voltage	V_{CC}					-0,5V +7,0V
2.2	Minimum and maximum input voltages						
2.2.1	Minimum and maximum input voltage	V_I					-0,5V +5,5V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}					+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	64S +85	74S +70	84S +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

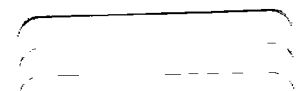
3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Maximum value of Low level output current for each output	I_{OLA}	All types	20,0	mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	All types	1,0	mA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54S 64/74/84S	0,3 0,5 0,7	V V V

3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)



3.2.1 (contd)

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IN} = 4,5V$ to all inputs Outputs enabled and open	V_{CC} max.	I_{CC}	-	74,0	mA
High level input current	$V_{IH(1)} = 5,5V$ $V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(1)}$	-	1,0	mA
			$I_{IH(2)}$	-	50,0	μA
Low level input current	$V_{IN} = 0,5V$	V_{CC} max.	$-I_{IL}$	-	2,0	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{IC}$	-	1,2	V
Output voltage	54S $-I_{OUT} = 1,0mA$ 64/74/84S $-I_{OUT} = 1,0mA$ All types $I_{OUT} = 20,0mA$ (1)	V_{CC} min.	V_{OH}	2,5	-	V
			V_{OH}	2,7	-	V
			V_{OL}	-	0,5	V
Output short circuit current	V_{IN} as required to give High output $V_O = 0V$ (2)	V_{CC} max.	$-I_{OS}$	40,0	100,0	mA

(1) Fan out = 10, (2) Only one output at a time, duration $t \leq 1s$

3.2.2 (contd)

Characteristics	Conditions	V _{CC} (V)	Symbol	Min.	Max.	Unit
Propagation times All types	T _{amb} = 25°C* test conditions as in Sub-group A5	5,0V				
High to Low level						
Binary select input to any output						
Non inverting inputs	(2 levels of delay)		t _{PHL}	-	10,5	ns
Inverting inputs	(3 levels of delay)		t _{PHL}	-	12,0	ns
Enable inputs to any output						
Non inverting inputs	(2 levels of delay)		t _{PHL}	-	11,0	ns
Inverting inputs	(3 levels of delay)		t _{PHL}	-	11,0	ns
Low to High level						
Binary select inputs to any output						
Non inverting inputs	(2 levels of delay)		t _{PLH}	-	7,0	ns
Inverting inputs	(3 levels of delay)		t _{PLH}	-	12,0	ns
Enable inputs to any output						
Non inverting inputs	(2 levels of delay)		t _{PLH}	-	8,0	ns
Inverting inputs	(3 levels of delay)		t _{PLH}	-	11,0	ns

*See Clauses 3.1 and 3.2.1 of this specification