

# BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002  
AND CECC 00 200 AND

BS CECC 90102 - 054

ISSUE 1

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## ELECTRONIC COMPONENTS OF ASSESSED QUALITY

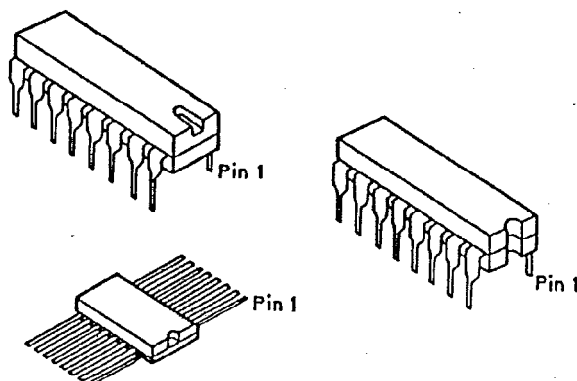
DETAIL SPECIFICATION IN ACCORDANCE WITH:

BS CECC 90 000 : 1976  
BS CECC 90 100 : 1977

## MANUFACTURERS TYPE NUMBER

54S162  
64S162  
74S162  
84S162

Outline not to scale: Isometric projection  
Marking information see clause 1



Refer to IEC 191-1-50a (type A50C)  
Dual-in-Line (plastic or ceramic)  
refer to Appendix A1.3  
Flatpack (metal or ceramic)

SEE PD 9002 AND CECC 00 200  
For ordering information see  
clause 1

4-BIT DECADE COUNTERS WITH  
SYNCHRONOUS CLEAR

TYPICAL CONSTRUCTION  
SILICON MONOLITHIC  
BIPOLAR CAVITY AND NON-  
CAVITY PACKAGES

ASSESSMENT LEVELS  
R, S, T AND V

### 1. Type description

#### 1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200  
for details of manufacturers approved to this specification

## 1.1 Truth table (contd)

| REMARKS                                                   | INPUTS |      |                                                           |   |   |   |        |   |       | OUTPUTS |                                                             |                |                |                |
|-----------------------------------------------------------|--------|------|-----------------------------------------------------------|---|---|---|--------|---|-------|---------|-------------------------------------------------------------|----------------|----------------|----------------|
|                                                           | CLEAR  | LOAD | DATA                                                      |   |   |   | ENABLE |   | CLOCK | CARRY   | Q <sub>D</sub>                                              | Q <sub>C</sub> | Q <sub>B</sub> | Q <sub>A</sub> |
|                                                           |        |      | D                                                         | C | B | A | T      | P |       |         |                                                             |                |                |                |
| Count 0<br>1<br>2                                         | L      | X    | X                                                         | X | X | X | X      | X | H     | L       | L                                                           | L              | L              | L              |
|                                                           | H      | H    | X                                                         | X | X | X | H      | H | H     | L       | L                                                           | L              | L              | L              |
|                                                           | H      | H    | X                                                         | X | X | X | H      | H | L     | L       | L                                                           | L              | L              | L              |
|                                                           | H      | H    | X                                                         | X | X | X | H      | H | ↑     | L       | L                                                           | L              | L              | H              |
|                                                           | H      | H    | X                                                         | X | X | X | H      | H | ↑     | L       | L                                                           | L              | H              | L              |
| These conditions are applied for a further 7 clock pulses |        |      |                                                           |   |   |   |        |   |       |         | Outputs follow binary count sequence to count of 9          |                |                |                |
| Count 9                                                   | H      | H    | X                                                         | X | X | X | H      | H | H     | H       | H                                                           | L              | L              | H              |
| No change                                                 | H      | L    | L                                                         | L | L | L | X      | X | H     | H       | H                                                           | L              | L              | H              |
| No change                                                 | H      | L    | L                                                         | L | L | L | X      | X | L     | H       | H                                                           | L              | L              | H              |
| Load 0                                                    | H      | L    | L                                                         | L | L | L | X      | X | ↑     | L       | L                                                           | L              | L              | L              |
| Load 1                                                    | H      | L    | L                                                         | L | L | H | X      | X | ↑     | L       | L                                                           | L              | L              | H              |
| Load 15                                                   | H      | L    | Binary inputs follow binary count sequence to count of 15 |   |   |   | X      | X | ↑     | L       | Outputs follow binary count sequence after each clock pulse |                |                |                |
|                                                           | H      | L    | H                                                         | H | H | H | X      | X | ↑     | L       | H                                                           | H              | H              | H              |
|                                                           | H      | H    | X                                                         | X | X | X | L      | H | ↑     | L       | H                                                           | H              | H              | H              |
|                                                           | H      | H    | X                                                         | X | X | X | L      | H | ↑     | L       | H                                                           | H              | H              | H              |
|                                                           | H      | H    | X                                                         | X | X | X | H      | L | L     | H       | H                                                           | H              | H              | H              |
| Unstable State                                            | H      | H    | X                                                         | X | X | X | H      | L | ↑     | H       | H                                                           | H              | H              | H              |

H = High level

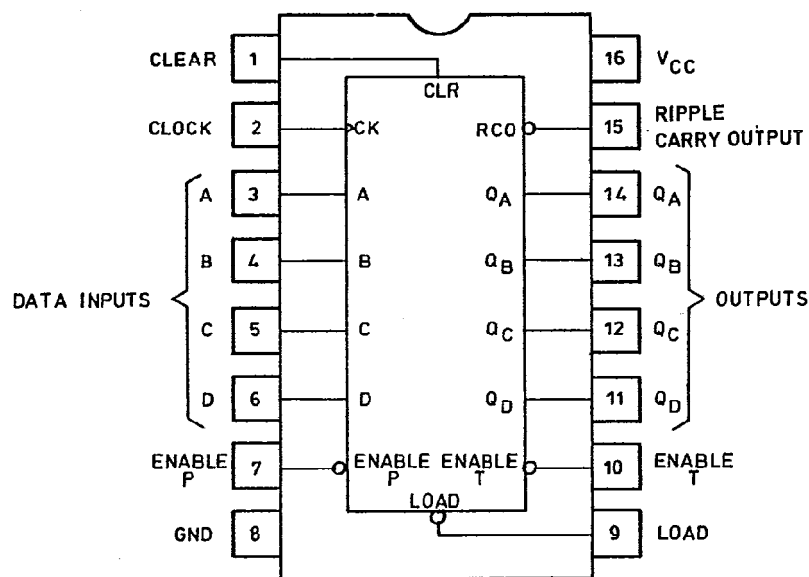
L = Low level

X = Logic level irrelevant

↑ = Positive clock transition

## 1.2 Terminal identification, type designation and marking

## 1.2.1 Terminal identification



## 4-bit decade counter with synchronous clear

The counter is a 4-bit decade counter incorporating a "Carry" circuit. Synchronous operation is provided by simultaneous clocking of the four D-type bistables, this arrangement causes the outputs to change coincident with each other when so ordered by the Count Enable inputs and internal gating. A buffered Clock input triggers the four bistables on its transition from Low to High.

Outputs may be preset by setting the Data inputs to the desired output levels whilst the Load input is Low, and taking the Clock from Low to High. During presetting, the levels of the Enable inputs are disregarded, and the Low at the load input disables the counter.

The "Carry" circuit allows counters to be cascaded without additional gating. The signals associated with this circuit are the two Count Enable inputs (P and T) and a Ripple Carry Output. When the counter reaches its maximum count with both Count Enable inputs High (both must be High for the counter to count), input T enables the Ripple Carry output which produces a High output pulse. This pulse can be used to enable succeeding cascaded stages.

## 1.2.1 Terminal identification (contd)

The clear function is synchronous. A Low at the Clear input sets all four bistable outputs Low after the next clock pulse regardless of the levels at the Enable inputs. This allows the count length to be easily modified.

## 1.2.2 Type designation

| TEMPERATURE<br>RANGE | PACKAGE                 |                         |                     |
|----------------------|-------------------------|-------------------------|---------------------|
|                      | Ceramic<br>Dual-in-Line | Plastic<br>Dual-in-Line | Ceramic<br>Flatpack |
| 0 + 70               | 74S162J                 | N                       | W                   |
| -25 + 85             | 84S162J                 |                         |                     |
| -40 + 85             | 64S162J                 |                         |                     |
| -55 +125             | 54S162J                 |                         |                     |

## 1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

## 1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1 Maximum continuous supply voltage  $V_{CC}$  -0,5V  
+7,0V

## 2.2 Maximum input voltages

2.2.1 Maximum input voltage  $V_I$  -0,5V  
+5,5V

2.2.2 Maximum input voltage between multiple emitter transistor inputs  $V_{II}$  +5,5V

|     |                                                    |                       | 54S  | 64S  | 74S         | 84S |     |
|-----|----------------------------------------------------|-----------------------|------|------|-------------|-----|-----|
| 2.3 | Minimum and maximum operating ambient temperatures | $T_{amb} (^{\circ}C)$ | min. | -55  | -40         | 0   | -25 |
|     |                                                    |                       | max. | +125 | +85         | +70 | +85 |
| 2.4 | Minimum and maximum storage temperatures           | $T_{stg} (^{\circ}C)$ | min. | -65  | (All types) |     |     |
|     |                                                    |                       | max. | +150 |             |     |     |

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

## 3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

| Description                                                                                        | Symbol               | Type                          | Value                    | Unit        |
|----------------------------------------------------------------------------------------------------|----------------------|-------------------------------|--------------------------|-------------|
| Positive supply voltage range                                                                      | $V_{CC}$             | 54S<br>64/74/84S              | 4,5 - 5,5<br>4,75 - 5,25 | V<br>V      |
| Minimum value of High level input voltage                                                          | $V_{IHB}$            | All types                     | 2,0                      | V           |
| Maximum value of High level input voltage                                                          | $V_{IHA}$            | All types                     | 5,5                      | V           |
| Minimum value of Low level input voltage                                                           | $V_{ILB}$            | All types                     | -0,3                     | V           |
| Maximum value of Low level input voltage                                                           | $V_{ILA}$            | All types                     | 0,8                      | V           |
| Maximum value of Low level output current for each output                                          | $I_{OLA}$            | All types                     | 20,0                     | mA          |
| Maximum value of output current for each output at $V_{OH}$                                        | $-I_{OHA}$           | All types                     | 1,0                      | mA          |
| D.C. noise margin<br>at Low level ( $V_{ILA} - V_{OLA}$ )<br>at High level ( $V_{OHB} - V_{IHB}$ ) | $V_{NL}$<br>$V_{NH}$ | All types<br>54S<br>64/74/84S | 0,3<br>0,5<br>0,7        | V<br>V<br>V |

### 3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (\*)

|                       | 54S  | 64S  | 74S | 84S |    |
|-----------------------|------|------|-----|-----|----|
| T <sub>amb</sub> min. | -55  | -40  | 0   | -25 | °C |
| T <sub>amb</sub> max. | +125 | +85  | +70 | +85 |    |
| V <sub>CC</sub> min.  | 4,5  | 4,75 |     |     | V  |
| V <sub>CC</sub> max.  | 5,5  | 5,25 |     |     |    |

| Characteristics                  | Conditions                                             | $V_{CC}(\text{V})$    | Symbol      | Min.  | Max.   | Unit          |
|----------------------------------|--------------------------------------------------------|-----------------------|-------------|-------|--------|---------------|
| Total supply current per package | All outputs open                                       | $V_{CC} \text{ max.}$ | $I_{CC}$    | -     | 160,0  | mA            |
| High level input current         | $V_{IH(1)} = 5,5\text{V}$<br>$V_{IH(2)} = 2,7\text{V}$ | $V_{CC} \text{ max.}$ | $I_{IH(1)}$ | -     | 1,0    | mA            |
| Other inputs                     |                                                        |                       | $I_{IH(2)}$ | -     | 50,0   | $\mu\text{A}$ |
| Enable T                         |                                                        |                       | $I_{IH(2)}$ | -10,0 | -200,0 | $\mu\text{A}$ |
| Low level input current          |                                                        |                       | $I_{IH(2)}$ | -10,0 | -200,0 | $\mu\text{A}$ |
| Low level input current          | $V_{IN} = 0,5\text{V}$                                 | $V_{CC} \text{ max.}$ | $-I_{IL}$   | -     | 4,0    | mA            |
| Enable T                         |                                                        |                       | $-I_{IL}$   | -     | 2,0    | mA            |
| Other inputs                     |                                                        |                       | $-I_{IL}$   | -     | 2,0    | mA            |
| Input clamping voltage           | $-I_{IC} = 18,0\text{mA}$                              | $V_{CC} \text{ min.}$ | $-V_{IC}$   | -     | 1,2    | V             |