

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90102 - 058

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ELECTRONIC COMPONENTS OF ASSESSED QUALITY

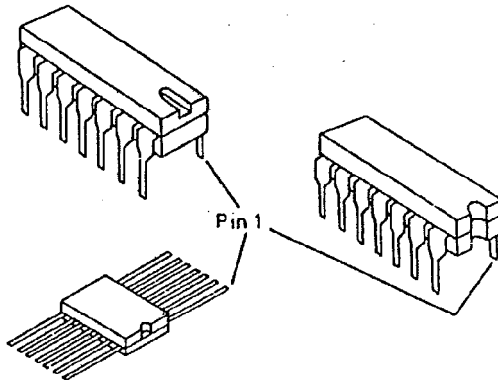
DETAIL SPECIFICATION IN ACCORDANCE WITH:

BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54S197
64S197
74S197
84S197

Outline not to scale: Isometric projection
Marking information see clause 1



Refer to IEC 191-1-50a (type A50B)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)

SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1

PRESETTABLE BINARY COUNTERS/ LATCHES

TYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR CAVITY AND NON-
CAVITY PACKAGES

ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table

CLOCK 1 COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = High level

L = Low level

Note Q_A connected to Clock 2 input

The counters each comprise four master-slave bistables which are internally connected to provide a divide-by-two and a divide-by-eight counter. The outputs (Q_A, Q_B, Q_C, Q_D) may be preset by taking the Count/Load input Low and presenting the required data at the Data input (A, B, C, D). The outputs change to agree with the Data inputs independent of the level of either Clock input.

For use as a 4-bit counter, output Q_A must be externally connected to Clock 2 input. Input count pulses are then applied to the Clock 1 input and simultaneous divisions by two, four, eight and sixteen are available at the output (see truth table).

For use as a 3-bit counter, the input count pulses are applied to the Clock 2 input and simultaneous divisions by two, four and eight are available at the Q_A, Q_C and Q_D outputs. Independent use of bistable A is available if the Load and Clear functions coincide with those of the three-bit counter.

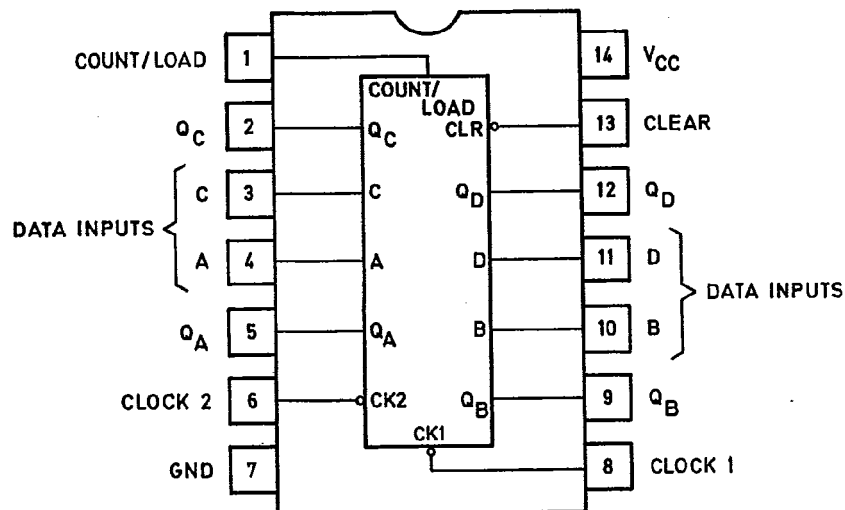
During counting, information is transferred to the outputs on the negative-going edge of the Clock pulse. Application of a Low to the direct Clear input sets all outputs Low regardless of the level of the Clocks.

The counters can be used as 4-bit latches by using the Count/Load input as the strobe and presenting data at the Data input. With the Count/Load Low, the outputs directly follow the Data inputs, but with the Count/Load High and the Clock input inactive, the outputs remain unchanged.

(For details of logic diagram see clause 3.3.4)

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Presettable binary counters/latches

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S197J	N	W
-25 + 85	84S197J		
-40 + 85	64S197J		
-55 +125	54S197J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Minimum and maximum continuous supply voltage	V_{CC}		-0,5V +7,0V
2.2	Minimum and maximum input voltages			
2.2.1	Minimum and maximum input voltage	V_I		-0,5V +5,5V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}		+5,5V
			54S 64S 74S 84S	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125
				-40 +85
				0 +70
				-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150
				(All types)

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V

3.1 (contd)

Description-	Symbol	Type	Value	Unit
Maximum value of Low level input voltage	V_{ILA}	54S 64/74/84S	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	All types	20,0	mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	All types	1,0	mA
D.C. noise margin				
at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54S 64/74/84S	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package 54S 64/74/84S	All outputs open circuit	$V_{CC} \text{ max.}$	I_{CC} I_{CC}	-	110,0 120,0	mA mA
High level input current	$V_{IH(1)} = 5,5V$ $V_{IH(2)} = 2,7V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$ $I_{IH(2)}$	-	1,0 50,0	mA μA
Low level input current Data, Count/Load Clear Clock 1 Clock 2	$V_{IN} = 0,5V$	$V_{CC} \text{ max.}$	I_{IL} I_{IL} I_{IL} I_{IL}	-	0,75 0,75 -8,0 -6,0	mA mA mA mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{IC}$	-	1,2	V
Output voltage 54S 64/74/84S All types	$-I_{OH} = 1,0mA$ $-I_{OH} = 1,0mA$ $I_{OL} = 20,0mA \text{ (1)}$	$V_{CC} \text{ min.}$	V_{OH} V_{OH} V_{OL}	2,5 2,7 -	- - 0,5	V V V
Output short circuit current	V_{IN} as defined by truth table to give High level output $V_O = 0V \text{ (2)}$	$V_{CC} \text{ max.}$	$-I_{OS}$	30,0	110,0	mA
Propagation times All types	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
High to Low level						
From To						
Clock 1 Q_A			t_{PHL}	-	10,0	ns
Clock 2 Q_B			t_{PHL}	-	12,0	ns
Clock 2 Q_C			t_{PHL}	-	22,0	ns
Clock 2 Q_D			t_{PHL}	-	33,0	ns
A/B/C/D $Q_A Q_B Q_C Q_D$			t_{PHL}	-	18,0	ns
Load Any output			t_{PHL}	-	18,0	ns
Clear Any output			t_{PHL}	-	37,0	ns

(1) Fan out = 10, (2) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See Clauses 3.1 and 3.2.1 of this specification