

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90102 - 059

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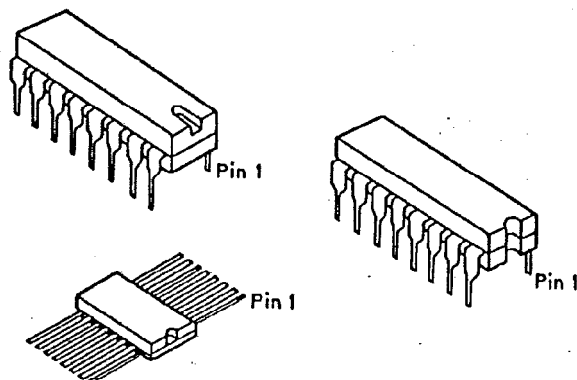
ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:

BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54S251
64S251
74S251
84S251

Outline not to scale: Isometric projection
Marking information see clause 1



Refer to IEC 191-1-50a (type A50C)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)

SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1

8-LINE TO 1-LINE DATA
SELECTOR/MULTIPLEXERS
WITH THREE LEVEL OUTPUTS

TYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR CAVITY AND NON-
CAVITY PACKAGES

ASSESSMENT LEVELS
R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A			
X	X	X	H	Z	<u>Z</u>
L	L	L	L	D0	<u>D0</u>
L	L	H	L	D1	<u>D1</u>
L	H	L	L	D2	<u>D2</u>
L	H	H	L	D3	<u>D3</u>
H	L	L	L	D4	<u>D4</u>
H	L	H	L	D5	<u>D5</u>
H	H	L	L	D6	<u>D6</u>
H	H	H	L	D7	<u>D7</u>

H = High level

L = Low level

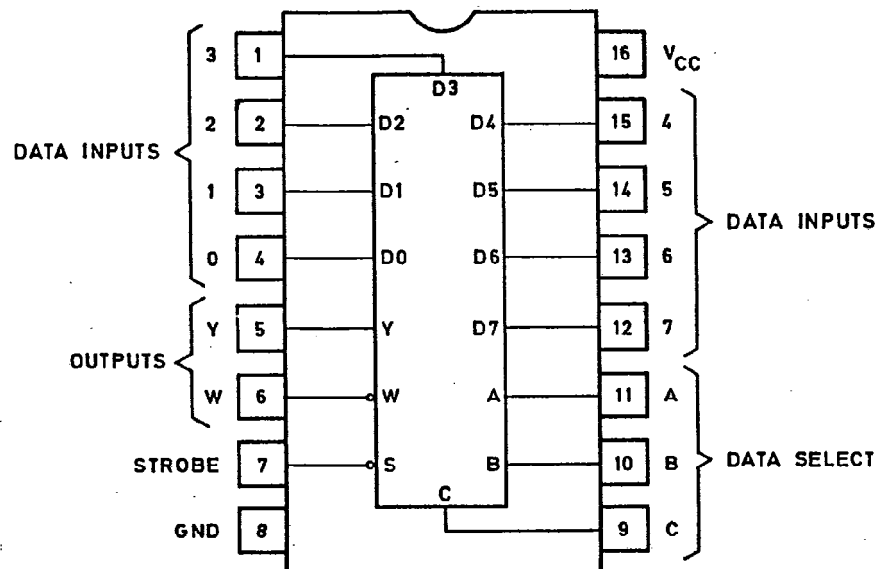
X = Level irrelevant

Z = High impedance level (output disabled)

D0, D1, ..., D7 = The level of the respective D input

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



8-line to 1-line data selector/multiplexers with three level output

1.2.1 Terminal identification (contd)

Three level device	A device whose output can be driven into a High, Low or high impedance level
High impedance level	That level of a device in which the output acquires a high impedance characteristic
High impedance leakage current	The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high impedance level

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S251J	N	W
-25 + 85	84S251J		
-40 + 85	64S251J		
-55 +125	54S251J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Minimum and maximum continuous supply voltage	V_{CC}					-0,5V +7,0V
2.2	Minimum and maximum input voltages						
2.2.1	Minimum and maximum input voltages	V_I					-0,5V +5,5V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}					+5,5V
	Maximum off level output voltage	V_O					+5,5V
				54S	64S	74S	84S
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Maximum value of Low level output current for each output	I_{OLA}	All types	20,0	mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	54S 64/74/84S	2,0 6,5	mA mA
High impedance level output current (leakage) $V_{OUT} = 2,4V$ $V_{OUT} = 0,5V$	I_{OHZ} $-I_{OLZ}$	All types All types	50,0 50,0	μA μA

3.1 (contd)

Description	Symbol	Type	Value	Unit
D.C. noise margin				
at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54S	0,5	V
		64/74/84S	0,7	V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current	4,5V to all inputs. All outputs open	V_{CC} max.	I_{CC}	-	85,0	mA
High level input current	$V_{IH(1)} = 5,5V$	V_{CC} max.	$I_{IH(1)}$	-	1,0	mA
	$V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(2)}$	-	50,0	µA
Low level input current	$V_{IN} = 0,5V$	V_{CC} max.	$-I_{IL}$	-	2,0	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	5,0V	$-V_{IC}$	-	1,2	V
Output voltage	All types All types $-I_{OUT} = I_{OHA}^*$ $I_{OUT} = I_{OLA}^* (1)$	V_{CC} min.	V_{OH}	2,4	-	V
			V_{OL}	-	0,5	V
Output short circuit current	Apply input according to table 1.1 to obtain High level output $V_O = 0V (3)$	V_{CC} max.	$-I_{OS}$	40,0	100,0	mA

(1) Fan out = 10, (2) To all inputs

(3) Only one output at a time, duration $t \leq 1s$

*See 3.2.1 of this specification

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Propagation times All types	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
High to Low level						
From To						
A, B or C Y	4 levels of delay		t_{PHL}	-	19,5	ns
A, B or C W	3 levels of delay		t_{PHL}	-	13,5	ns
Any data input Y			t_{PHL}	-	12,0	ns
Any data input W			t_{PHL}	-	7,0	ns
Low to High level						
From To						
A, B or C Y	4 levels of delay		t_{PLH}	-	18,0	ns
A, B or C W	3 levels of delay		t_{PLH}	-	15,0	ns
Any data input Y			t_{PLH}	-	12,0	ns
Any data input W			t_{PLH}	-	7,0	ns
Output enable to High level	Strobe to Y or W		t_{PZH}	-	19,5	ns
Output enable to Low level	Strobe to Y or W		t_{PZL}	-	21,0	ns
Output disable from High level	Strobe to Y or W		t_{PHZ}	-	8,5	ns
Output disable from Low level	Strobe to Y or W		t_{PLZ}	-	14,0	ns