

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90102 - 062

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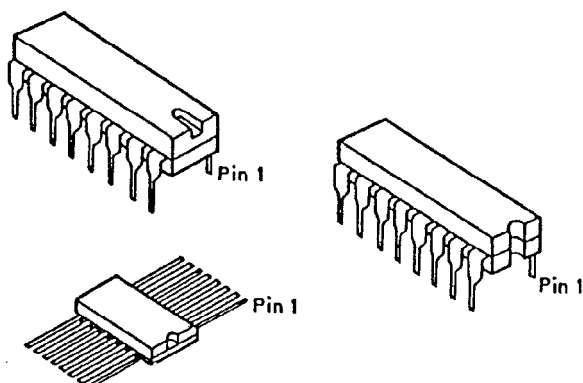
ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:

BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54S280
64S280
74S280
84S280

Outline not to scale: Isometric projection
Marking information see clause 1



Refer to IEC 191-1-50a (type A50C)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)

SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1

9-BIT ODD/EVEN PARITY
GENERATORS/CHECKERS

TYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR CAVITY AND NON-
CAVITY PACKAGES

ASSESSMENT LEVELS
R, S, T AND V

1. Type description

1.1 Truth table

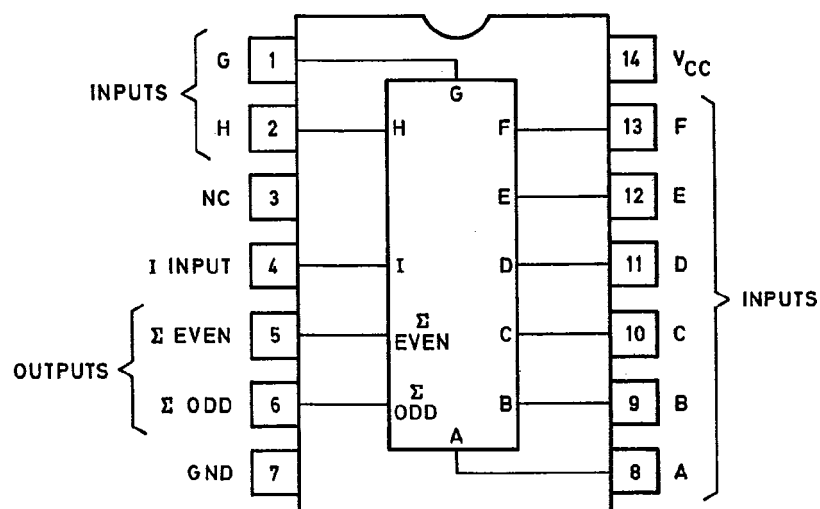
NUMBER OF INPUTS THAT ARE HIGH (A through I)	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = High level
L = Low level

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



9-bit odd/even parity generator/checker

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S280J	N	W
-25 + 85	84S280J		
-40 + 85	64S280J		
-55 +125	54S280J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Minimum and maximum continuous supply voltages	V_{CC}						-0,5V +7,0V
2.2	Minimum and maximum input voltages							
2.2.1	Minimum and maximum input voltage	V_I						-0,5V +5,5V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
					54S	64S	74S	84S
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

3.1 (contd)

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	0	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Maximum value of Low level output current	I_{OLA}	All types	20,0	mA
Maximum value of High level output current	$-I_{OHA}$	All types	1,0	mA
D.C. noise margin				
at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54S	0,5	V
	V_{NH}	64/74/84S	0,7	V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	54S	$V_{CC} \text{ max.}$	I_{CC}	-	99,0	mA
	64/74/84S		I_{CC}	-	105,0	mA
High level input current	$V_{IH(1)} = 5,5V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	1,0	mA
	$V_{IH(2)} = 2,7V$	$V_{CC} \text{ max.}$	$I_{IH(2)}$	-	50,0	μA
Low level input current	$V_{IN} = 0,5V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	2,0	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{IC}$	-	1,2	V
Output voltage	54S $V_{IN} = 0,8V$ and/or $2,0V$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
	64/74/84S $-I_{OH} = I_{OHA}$		V_{OH}	2,7	-	V
	All types $I_{OL} = I_{OLA}^* (1)$		V_{OL}	-	0,5	V
Output short circuit current	V_{IN} to give High level output $V_O = 0V (2)$	$V_{CC} \text{ max.}$	$-I_{OS}$	40,0	100,0	mA
Propagation times	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
All types						
High to Low level						
From	To					
Data	Σ Even		t_{PHL}	-	18,0	ns
Data	Σ Odd		t_{PHL}	-	18,0	ns
Low to High level						
From	To					
Data	Σ Even		t_{PLH}	-	21,0	ns
Data	Σ Odd		t_{PLH}	-	21,0	ns

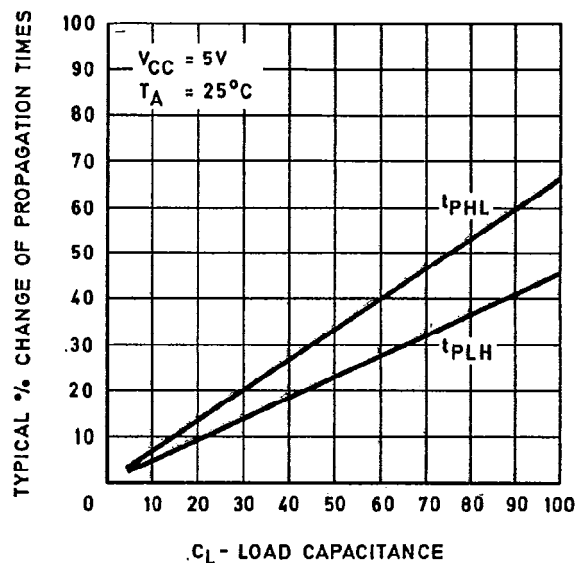
(1) Fan out = 10,

(2) Only one output at a time, duration $t \leq 1s$

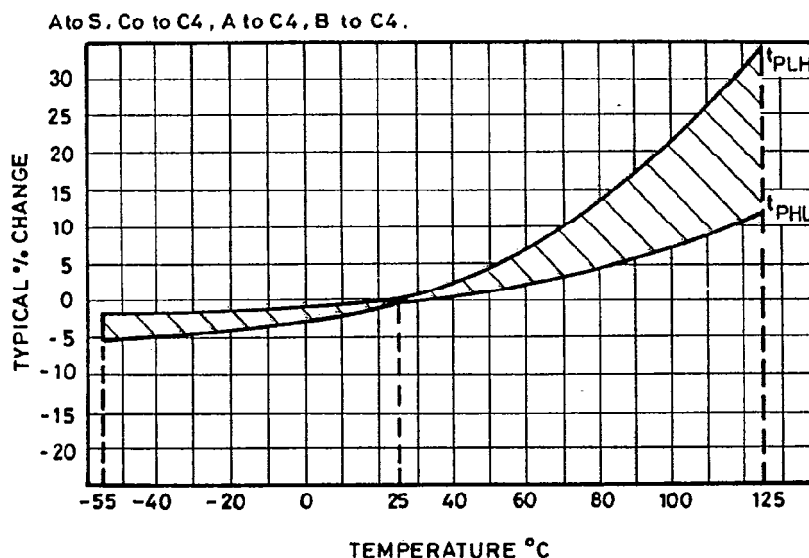
*See Clauses 3.1 and 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



3.3.2 Variation of propagation time with temperature



3.3.3 Gates

Inputs of unused gates should be connected in such a way that the output is set to High level to ensure minimum power dissipation.

3.4 Typical values* ($V_{CC} = 5.0V$, $T_{amb} = 25^\circ C$)

typical supply current of the device (50% duty cycle)

$$S280 \quad I_{CC} = 67,0mA$$

Typical propagation time:

$$S280 \quad t_{Ptyp} = \frac{t_{PHL} + t_{PLH}}{2} = 19,5ns \text{ (Data to } \Sigma \text{ Even)}$$

*See 3.2 of this specification