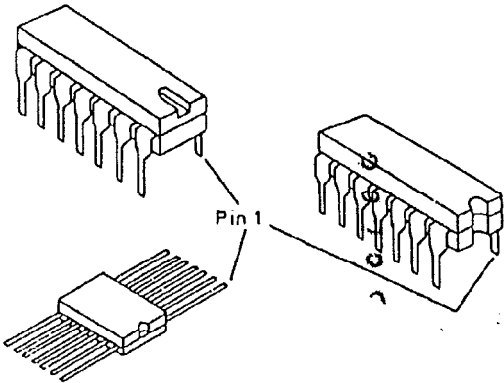


BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON, W1A 2BS	BS CECC 90102-063 ISSUE 1, MAY 1983  Page 1 of 17 Pages
Specification available from:— AS SHOWN IN PD 9002 AND CECC 00 200 AND TEXAS INSTRUMENTS LIMITED, MANTON LANE, BEDFORD, MK41 7PA	MANUFACTURER'S TYPE NUMBER 54S51 64S51 74S51 84S51 SEE PD 9002 AND CECC 00200 For ordering information see Clause 1
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH BS CECC 90 000 : 1982 BS CECC 90 100 : 1977 Outline not to scale: Isometric projection. Marking information see Clause 1  Refer to IEC 191-1-50a (type A50B), Dual-in-line (Plastic or Ceramic). Refer to Appendix A1.3, Flatpack (Metal or Ceramic)	DUAL 2-WIDE 2-INPUT AND-OR- INVERT GATES TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR CAVITY AND NON- CAVITY PACKAGES ASSESSMENT LEVELS R, S, T AND V

1. Type Description

1.1 Truth Table (See Page 2)

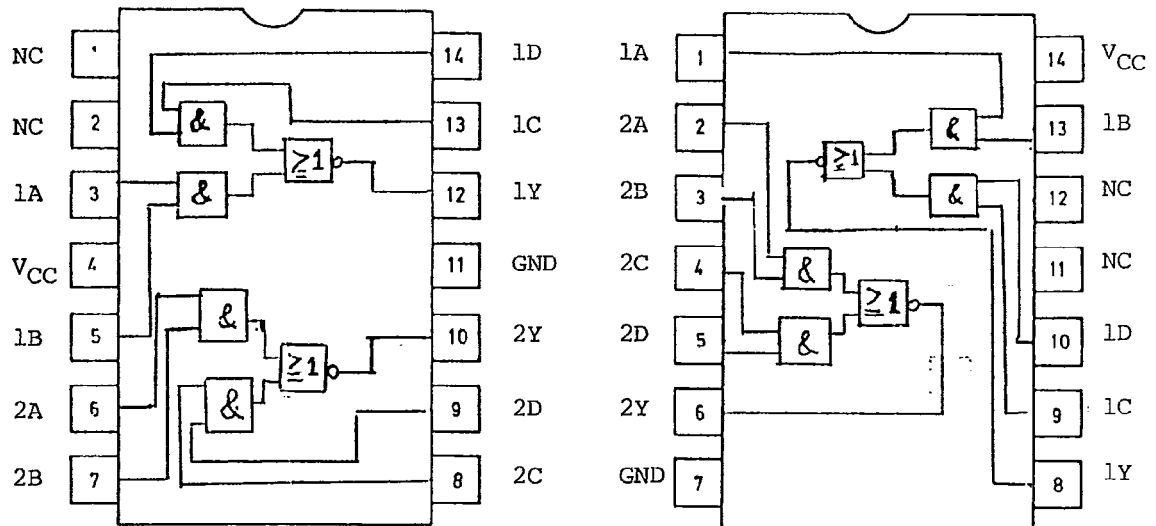
Refer to Qualified Products List PD 9002 and/or CECC 00200 for details of manufacturers approved to this specification.

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1.1. (Cont'd)

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	L
L	H	L	L	H
L	H	L	H	H
L	H	H	L	H
L	H	H	H	L
H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	L

1.2. Terminal identification, type designation and marking

1.2.1. Terminal Identification

Quadruple 2-input positive Nor gates

1.2.2. Type Designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S51J	N	S
-25 + 85	84S51J		
-40 + 85	64S51J		
-55 +125	54S54J		

1.2.3. Marking

Each integrated circuit shall bear the following marking:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

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1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Minimum and maximum continuous supply voltage	V_{CC}		-0,5V +7,0V
2.2	Minimum and maximum input voltages			
2.2.1	Minimum and maximum input voltage	V_I		-0,5V +5,5V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}		+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	54S 64S 74S 84S -40 0 -25 +85 +70 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the full operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54S 64/74/84S	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	All types	0,8	V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IIA}	54S 64/74/84S	5,0 5,25	V V

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum value of Low level output current for each output	I_{OLA}	All types	20.0	mA
Maximum value of High level output current	$-I_{OHA}$	All types	1000.0	μA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0.3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54S	0.5	V
	V_{NH}	64/74/84S	0.7	V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation within the ambient temperature range, except for those conditions marked with an asterisk (*).

	54S	64S	74S	84S	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current at High level	Apply input conditions to give High level output	V_{CC} max.	I_{CCH}	-	17.8	mA
Total supply current at Low level	Apply input conditions to give Low level output	V_{CC} max.	I_{CCL}	-	22.0	mA
High level input current	$V_{IN} = 5,5V^{(1)}$	V_{CC} max.	$I_{IH(1)}$	-	1,0	mA
	$V_{IN} = 2,7V^{(1)}$		$I_{IH(2)}$	-	50,0	μA

(1) To all inputs

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Low level input current	$V_{IN} = 0,5V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	2,0	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{IC}$	-	1,2	V
Output voltage 54S 64/74/84S	$I_{OL} = 20,0mA^{(2)}$ $-I_{OH} = 1,0mA$	$V_{CC} \text{ min.}$	V_{OL} V_{OH} V_{OH}	- 2,5 2,7	0,5 - -	V V V
Output short circuit current	$V_O = 0V^{(3)}$	$V_{CC} \text{ max.}$	$-I_{OS}$	40,0	100,0	mA
Propagation time	$T_{amb} = 25^{\circ}C^{*}$ test conditions as in Sub-group A5	5,0V				
Low to High level			t_{PLH}	-	5,5	ns
High to Low level			t_{PHL}	-	5,5	ns

(2) Fan out = 10

(3) Only one output at a time, duration $t \leq 1s$

*See Clauses 3.1 and 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading

