

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

BS CECC 90103 - 027

ISSUE 1

June 1981



Page 1 of 17 pages

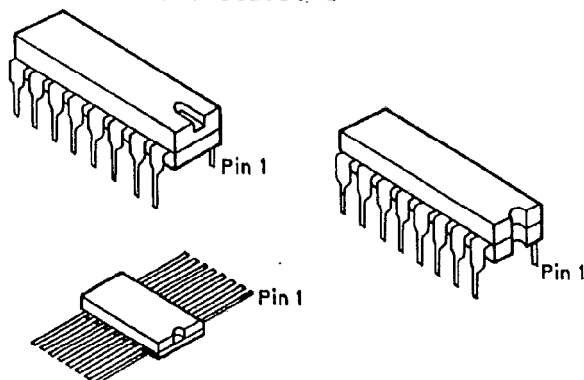
ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:

BS CECC 90 000 : 1976
 BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54S158
 64S158
 74S158
 84S158

Outline not to scale: Isometric projection
Marking information see clause 1



Refer to IEC 191-1-50a (type A50C)
 Dual-in-Line (plastic or ceramic)
 refer to Appendix A1.3
 Flatpack (metal or ceramic)

SEE PD 9002 AND CECC 00 200
 For ordering information see
 clause 1

**QUADRUPLE 2-LINE-TO-1-LINE
 DATA SELECTOR/MULTIPLEXERS**

TYPICAL CONSTRUCTION
SILICON MONOLITHIC BIPOLAR
CAVITY AND NON-CAVITY
PACKAGES

ASSESSMENT LEVELS
 R, S, T, AND V

1. Type description

1.1 Truth table

INPUTS				OUTPUT
STROBE	SELECT	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level

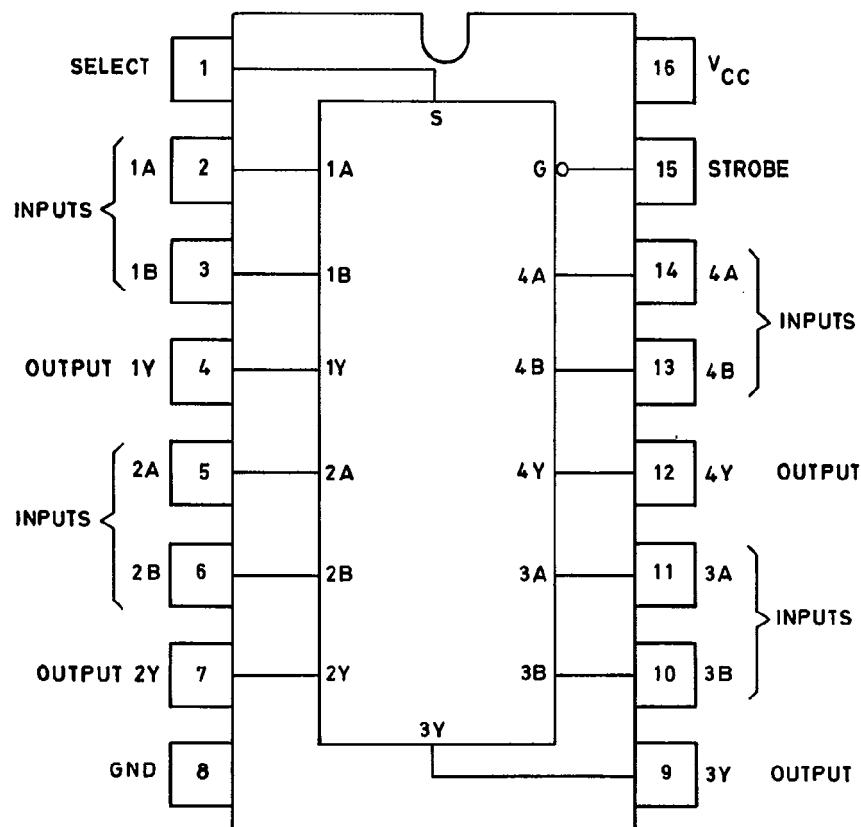
L = Low level

X = Logic level irrelevant

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Quadruple 2-line to 1-line data selector/multiplexers

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74S158J	N	W
-25 + 85	84S158J		
-40 + 85	64S158J		
-55 +125	54S158J		

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS42J	N	W
-25 + 85	84LS42J		
-40 + 85	64LS42J		
-55 +125	54LS42J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	54LS -55 +125	64LS -40 +85	74LS 0 +70	84LS -25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OL}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OH}	All types	-400,0	μ A

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T_{amb} min.	-55	-40	0	-25	°C
T_{amb} max.	+125	+85	+70	+85	
V_{CC} min.	4,5	4,75			V
V_{CC} max.	5,5	5,25			

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IN} = 0V$ (1)	$V_{CC} \text{ max.}$	I_{CC}	-	13,0	mA
High level input current	$V_{IH(1)} = 7,0V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	100,0	μA
	$V_{IH(2)} = 2,7V$	$V_{CC} \text{ max.}$	$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ max.}$	$-V_{ICA}$	-	1,5	V
Output voltage. 54LS 64/74/84LS	$I_{OH} = -400,0\mu A$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
	$I_{OL(1)} = 4,0mA$ (2)		$V_{OL(1)}$	-	0,4	V
	$I_{OL(2)} = 8,0mA$ (3)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ (4)	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times All types	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
From any input through 2 levels of logic			t_{PLH}	-	25,0	ns
From any input through 3 levels of logic				-	30,0	ns
From any input through 2 levels of logic			t_{PHL}	-	25,0	ns
From any input through 3 levels of logic				-	30,0	ns

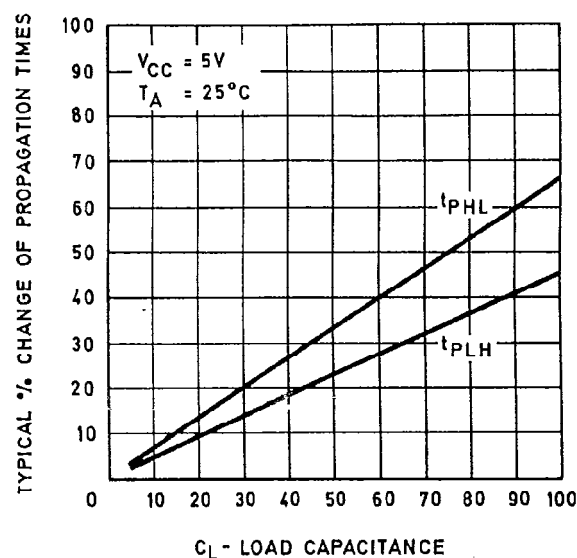
(1) To all inputs, (2) Fan out = 10, (3) Fan out = 20,

(4) Only one input at a time, duration $t \leq 1 \text{ sec}$

* See 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation time Vs. load capacitance

3.3.2 Variation of propagation time with temperature

