

BRITISH STANDARDS INSTITUTION, 2 PARK STREET, LONDON, W1A 2BS	Page 1 of 17	CECC 90103 - 030 ISSUE 1 NOVEMBER 1981
ELECTRONIC COMPONENTS OF ASSESSED QUALITY IN ACCORDANCE WITH: BS CECC 90 000 BS CECC 90 100 and family specification for TTL Low-Power-Schottky-circuits (BS CECC 90103)	BS CECC 90103 - 030 ISSUE 1 NOVEMBER 1981	
Detail specification for 2-wide 3-input, 2-wide 2-input And-Or-invert gates		
Device types: 54LS51 64LS51 74LS51 84LS51		
TYPICAL CONSTRUCTION Silicon monolithic bipolar TTL Low-Power-Schottky		
Outline and dimensions Refer to IEC 191 1-50a type A 50 B Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	Assessment levels R, S, T, V	

1. Type description

1.1 Truth table (see page 2)

See relevant Qualified Products List for the availability
of components qualified to this detail specification

1.1 Truth table (contd)

INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
L	X	X	L	X	X	H
L	X	X	X	L	X	H
L	X	X	X	X	L	H
X	L	X	L	X	X	H
X	L	X	X	L	X	H
X	L	X	X	X	L	H
X	X	L	L	X	X	H
X	X	L	X	L	X	H
X	X	L	X	X	L	H
X	X	X	H	H	H	L
H	H	H	X	X	X	L

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
X	X	H	H	L
H	H	X	X	L

H = High level
 L = Low level
 X = Logic level irrelevant

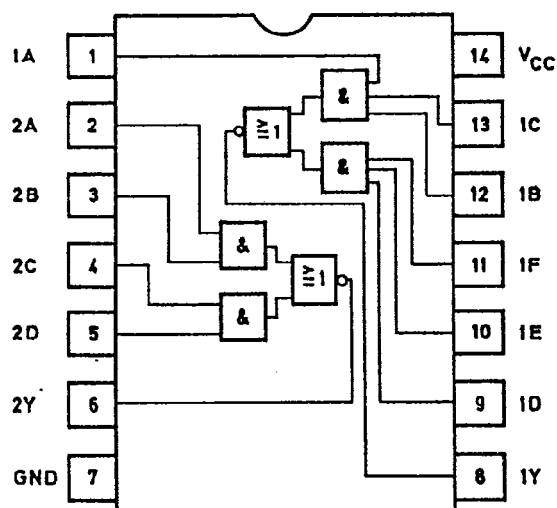
1.1.1 Boolean equation

$$1Y = \overline{(1A, 1B, 1C)} + (1D, 1E, 1F)$$

$$2Y = \overline{(2A, 2B)} + (2C + 2D)$$

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



2-wide 3-input, 2-wide 2-input
And-Or-invert gates

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flat pack
0 + 70	74LS51J	N	W
-25 + 85	84LS51J		
-40 + 85	64LS51J		
-55 +125	54LS51J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage							-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
				54LS	64LS	74LS	84LS	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V

Description	Symbol	Type	Value	Unit
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	All types	400,0	μA

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current with High level output	$V_{IL} = 0V$ (1)	V_{CC} max.	I_{CCH}	-	1,6	mA
Total supply current with Low level output	$V_{IH} = 4,5V$	V_{CC} max.	I_{CCL}	-	2,8	mA
High level input current	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	100,0	μA
	$V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V

(1) To all inputs

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output voltage						
54LS	$I_{OH} = -400,0\mu A$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
64/74/84LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
All types	$I_{OL(1)} = 4,0mA^{(2)}$		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA^{(3)}$		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V^{(4)}$	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times	$T_{amb} = 25^\circ C^*$	5,0V	t_{PLH}	-	20,0	ns
All types	test conditions as in Sub-group A5		t_{PHL}	-	20,0	ns

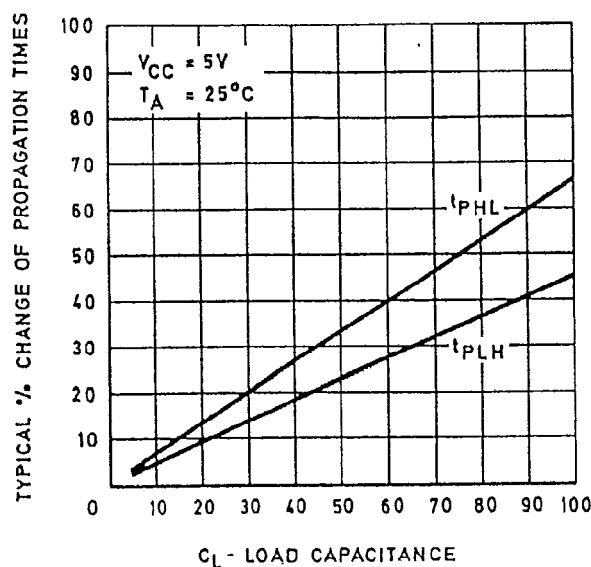
(2) Fan out = 10, (3) Fan out = 20,

(4) Only one output at a time, duration $t \leq 1 \text{ sec}$

* See 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance