

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90103 - 034

ISSUE 1

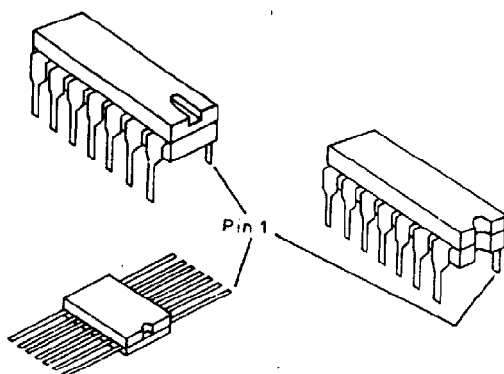
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ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54LS74A
64LS74A
74LS74A
84LS74AOutline not to scale: Isometric projection
Marking information see clause 1Refer to IEC 191-1-50a (type A50B)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1DUAL D-TYPE POSITIVE-EDGE
TRIGGERED BISTABLE WITH
PRESET AND CLEARTYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR TTL-LOW-POWER
SCHOTTKYASSESSMENT LEVELS
R, S, T AND V1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)
(each bistable)

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

* = This condition is unstable, and will not persist when preset and clear inputs return to their inactive (High level)

↑ = Positive transition from Low to High of the clock pulse

Q_0 = Q output before the indicated steady-level input conditions were established

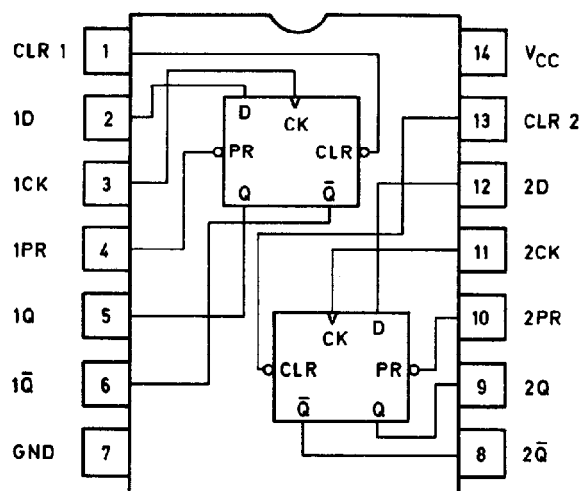
H = High level

L = Low level

X = Logic level irrelevant

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Dual D-type positive edge triggered
bistables with preset and clear

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS74AJ	N	W
-25 + 85	84LS74AJ		
-40 + 85	64LS74AJ		
-55 +125	54LS74AJ		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}					-0,5V +7,0V
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I					-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}					+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)		
				54LS	64LS	74LS	84LS

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μ A

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IL} = 0V$ (1)	$V_{CC} \text{ max.}$	I_{CC}	-	8,0	mA
High level input current	$V_{IH(1)} = 7,0V$ $V_{IH(2)} = 2,7V$	$V_{CC} \text{ max.}$ $V_{CC} \text{ max.}$	$I_{IH(1)}$ $I_{IH(2)}$	- - - -	0,1 0,2 0,2 0,1	mA mA mA mA
D, J or K Clear Preset Clock						
D, J or K Clear Preset Clock				- - - -	20,0 40,0 40,0 20,0	μA μA μA μA
Low level input current	$V_{IL} = 0,4V$	$V_{CC} \text{ max.}$	$-I_{IL}$	- - - -	0,4 0,8 0,8 0,4	mA mA mA mA
D, J or K Clear Preset Clock						
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage	$I_{OH} = -400,0\mu A$ $I_{OH} = -400,0\mu A$ All types $I_{OL(1)} = 4,0mA$ (2) 64/74/84LS $I_{OL(2)} = 8,0mA$ (3)	$V_{CC} \text{ min.}$	V_{OH} V_{OH} $V_{OL(1)}$ $V_{OL(2)}$	2,5 2,7 - -	- - 0,4 0,5	V V V V
Output short circuit current	$V_O = 0V$ (4)	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation time	$T_{amb} = 25^{\circ}C$ test conditions as in Sub-group A5	5,0V				
All types						
From Clear, preset or Clock (as appropriate)	To Q or $\bar{Q}$		t_{PHL}	-	40,0	ns
From Clear, preset or Clock (as appropriate)	To Q or $\bar{Q}$		t_{PLH}	-	25,0	ns

(1) To all inputs, (2) Fan out = 10, (3) Fan out = 20,

(4) Only one output at a time, duration $t \leq 1 \text{ sec}$

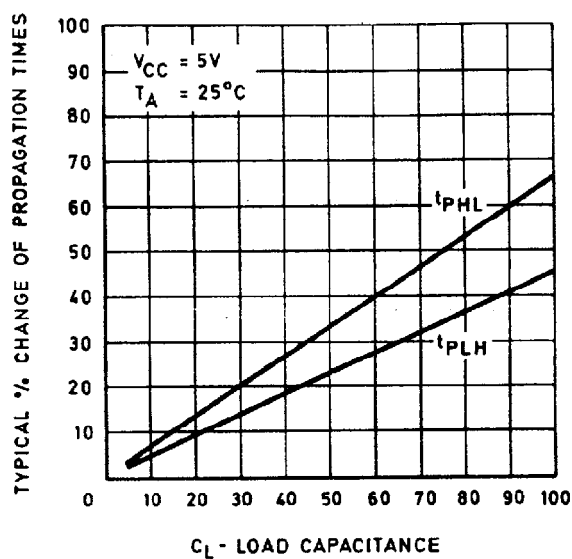
* See 3.2.1 of this specification

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Maximum Clock frequency			$f_{(clock)}$	25,0	-	MHz
Duration of Clock pulse			$t_{p(clock)}$	25,0	-	ns
Duration of Preset pulse			$t_{p(preset)}$	25,0	-	ns
Duration of Clear pulse			$t_{p(clear)}$	25,0	-	ns
Minimum set-up time High level data Low level data			t_{set-up} t_{set-up}	20,0 20,0	- -	ns ns
Data hold time			t_{Hold}	5,0	-	ns

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance