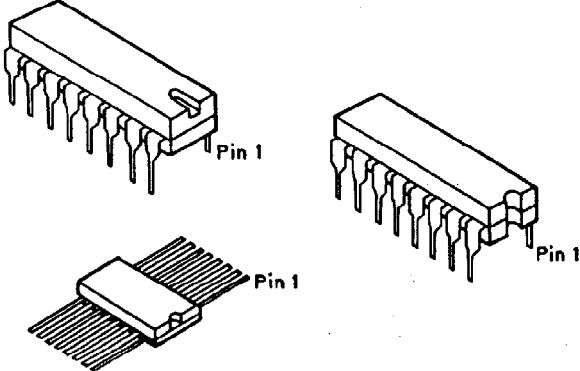




|                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                   |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p><b>BRITISH STANDARDS INSTITUTION</b><br/>2 PARK STREET, LONDON. W1A 2BS</p> <p>Specification available from:- AS SHOWN IN PD 9002<br/>AND CECC 00 200 AND</p>                                                                                                                                                                   | <p>BS CECC 90103 - 035</p> <p>ISSUE 1</p> <p>AUGUST 1981</p> <p>Page 1 of 19 pages</p>                                                                                                         |
| <p><b>ELECTRONIC COMPONENTS OF ASSESSED QUALITY</b><br/><b>DETAIL SPECIFICATION IN ACCORDANCE WITH:</b></p> <p>BS CECC 90 000 : 1976<br/>BS CECC 90 100 : 1977</p>                                                                                                                                                                 | <p><b>MANUFACTURERS TYPE NUMBER</b></p> <p>54LS75<br/>64LS75<br/>74LS75<br/>84LS75</p>                                                                                                                                                                                            |
| <p><b>Outline not to scale: Isometric projection</b><br/><b>Marking information see clause 1</b></p>  <p>Refer to IEC 191-1-50a (type A50C)<br/>Dual-in-Line (plastic or ceramic)<br/>refer to Appendix A1.3<br/>Flatpack (metal or ceramic)</p> | <p>SEE PD 9002 AND CECC 00 200<br/>For ordering information see<br/>clause 1</p> <p><b>DUAL 2-BIT BISTABLE<br/>LATCHES</b></p> <p><b>TYPICAL CONSTRUCTION</b><br/>SILICON MONOLITHIC<br/>BIPOLAR TTL-LOW-POWER<br/>SCHOTTKY</p> <p><b>ASSESSMENT LEVELS</b><br/>R, S, T AND V</p> |

# 1. Type description

## 1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200  
for details of manufacturers approved to this specification

1.1 Truth table (contd)  
(each bistable latch)

| INPUTS |   | OUTPUTS |             |
|--------|---|---------|-------------|
| D      | G | Q       | $\bar{Q}$   |
| L      | H | L       | H           |
| H      | H | H       | L           |
| X      | L | $Q_0$   | $\bar{Q}_0$ |

H = High level

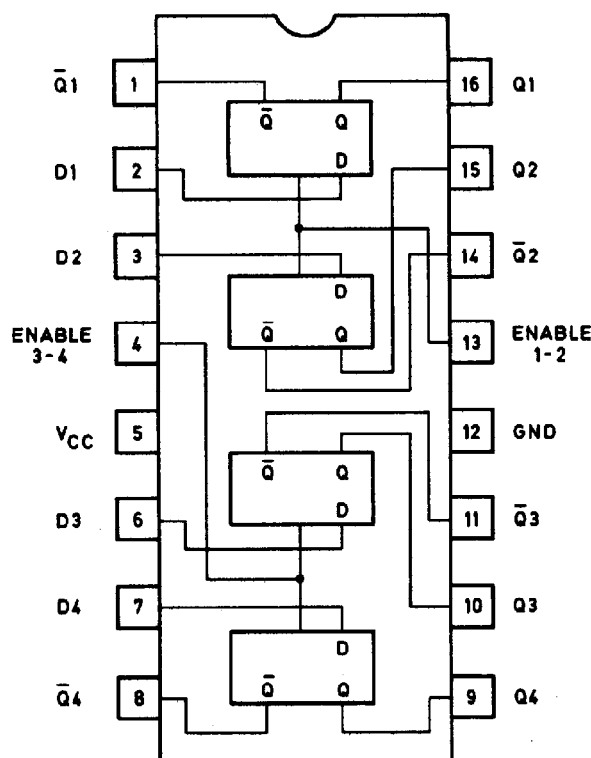
L = Low level

X = Logic level irrelevant

$Q_0, \bar{Q}_0$  = The level of Q and  $\bar{Q}$  before the indicated steady level input conditions

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Dual 2-bit bistable latches

## 1.2.2 Type designation

| TEMPERATURE<br>RANGE | PACKAGE                 |                         |                     |
|----------------------|-------------------------|-------------------------|---------------------|
|                      | Ceramic<br>Dual-in-Line | Plastic<br>Dual-in-Line | Ceramic<br>Flatpack |
| 0 + 70               | 74LS75J                 | N                       | W                   |
| -25 + 85             | 84LS75J                 |                         |                     |
| -40 + 85             | 64LS75J                 |                         |                     |
| -55 +125             | 54LS75J                 |                         |                     |

## 1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

## 1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

## 2. Limiting conditions of use (not for inspection purposes)

2.1 Maximum continuous supply voltage  $V_{CC}$  -0,5V  
+7,0V

2.2 Maximum input voltages

2.2.1 Maximum input voltage  $V_I$  -0,5V  
+7,0V

2.2.2 Maximum input voltage between multiple emitter transistor inputs  $V_{II}$  +5,5V

|     |                                                    |                      |                       |            |          |            |
|-----|----------------------------------------------------|----------------------|-----------------------|------------|----------|------------|
|     |                                                    |                      | 54LS                  | 64LS       | 74LS     | 84LS       |
| 2.3 | Minimum and maximum operating ambient temperatures | $T_{amb}(^{\circ}C)$ | min. -55<br>max. +125 | -40<br>+85 | 0<br>+70 | -25<br>+85 |

|     |                                          |                      |                       |             |
|-----|------------------------------------------|----------------------|-----------------------|-------------|
| 2.4 | Minimum and maximum storage temperatures | $T_{stg}(^{\circ}C)$ | min. -65<br>max. +150 | (All types) |
|-----|------------------------------------------|----------------------|-----------------------|-------------|

### 3. Recommended operating conditions and associated characteristics (not for inspection purposes)

#### 3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

| Description                                                 | Symbol    | Type               | Value                    | Unit     |
|-------------------------------------------------------------|-----------|--------------------|--------------------------|----------|
| Positive supply voltage range                               | $V_{CC}$  | 54LS<br>64/74/84LS | 4,5 - 5,5<br>4,75 - 5,25 | V<br>V   |
| Minimum value of High level input voltage                   | $V_{IHB}$ | All types          | 2,0                      | V        |
| Maximum value of High level input voltage                   | $V_{IHA}$ | All types          | 5,5                      | V        |
| Minimum value of Low level input voltage                    | $V_{ILB}$ | All types          | -0,3                     | V        |
| Maximum value of Low level input voltage                    | $V_{ILA}$ | 54LS<br>64/74/84LS | 0,7<br>0,8               | V<br>V   |
| Maximum value of Low level output current for each output   | $I_{OLA}$ | 54LS<br>64/74/84LS | 4,0<br>8,0               | mA<br>mA |
| Maximum value of output current for each output at $V_{OH}$ | $I_{OHA}$ | All types          | -400,0                   | $\mu A$  |
| D.C. noise margin<br>at Low level ( $V_{ILA} - V_{OLA}$ )   | $V_{NL}$  | All types          | 0,3                      | V        |
| at High level ( $V_{OHB} - V_{IHB}$ )                       | $V_{NH}$  | 54LS<br>64/74/84LS | 0,5<br>0,7               | V<br>V   |

#### 3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (\*)

## 3.2.1 (contd)

|                       | 54LS | 64LS | 74LS | 84LS |    |
|-----------------------|------|------|------|------|----|
| T <sub>amb</sub> min. | -55  | -40  | 0    | -25  | °C |
| T <sub>amb</sub> max. | +125 | +85  | +70  | +85  |    |
| V <sub>CC</sub> min.  | 4,5  | 4,75 |      |      | V  |
| V <sub>CC</sub> max.  | 5,5  | 5,25 |      |      |    |

## 3.2.2

| Characteristics                  | Conditions                                   | $V_{CC}(\text{V})$    | Symbol      | Min. | Max. | Unit          |
|----------------------------------|----------------------------------------------|-----------------------|-------------|------|------|---------------|
| Total supply current per package | 0V to all inputs<br>Outputs open circuit     | $V_{CC} \text{ max.}$ | $I_{CC}$    | -    | 12,0 | mA            |
| High level input current         | $V_{IH(1)} = 7,0\text{V}$                    | $V_{CC} \text{ max.}$ |             |      |      |               |
|                                  | D input                                      |                       | $I_{IH(1)}$ | -    | 0,1  | mA            |
|                                  | G input                                      |                       | $I_{IH(1)}$ | -    | 0,4  | mA            |
|                                  | $V_{IH(2)} = V_{OHB}$                        |                       |             |      |      |               |
|                                  | D input                                      |                       | $I_{IH(2)}$ | -    | 20,0 | $\mu\text{A}$ |
| Low level input current          | G input                                      | $V_{CC} \text{ max.}$ | $I_{IH(2)}$ | -    | 80,0 | $\mu\text{A}$ |
|                                  | $V_{IL} = 0,4\text{V}$ to each input in turn |                       |             |      |      |               |
|                                  | D input                                      |                       | $-I_{IL}$   | -    | 0,4  | mA            |
|                                  | G input                                      |                       | $-I_{IL}$   | -    | 1,6  | mA            |
|                                  |                                              |                       |             |      |      |               |
| Input clamping voltage           | $-I_{IC} = 18,0\text{mA}$                    | $V_{CC} \text{ min.}$ | $-V_{ICA}$  | -    | 1,5  | V             |

### 3.2.2 (contd)

| Characteristics              | Conditions                                                              | $V_{CC}(V)$    | Symbol            | Min. | Max.  | Unit |
|------------------------------|-------------------------------------------------------------------------|----------------|-------------------|------|-------|------|
| Output voltage               | $V_{IN} = V_{ILA}$ or 2,0V as appropriate.<br>Test each output in turn. | $V_{CC}$ min.  |                   |      |       |      |
| 54LS                         | $I_{OH} = -400,0\mu A$                                                  |                | $V_{OH}$          | 2,5  | -     | V    |
| 64/74/84LS                   | $I_{OH} = -400,0\mu A$                                                  |                | $V_{OH}$          | 2,7  | -     | V    |
| All types                    | $I_{OL(1)} = 4,0mA$ (1)                                                 |                | $V_{OL(1)}$       | -    | 0,4   | V    |
| 64/74/84LS                   | $I_{OL(2)} = 8,0mA$ (2)                                                 |                | $V_{OL(2)}$       | -    | 0,5   | V    |
| Output short circuit current | $V_{IN} = 0V$ or 4,5V as appropriate<br>$V_O = 0V$ (3)                  | $V_{CC}$ max.  | $-I_{OS}$         | 15,0 | 130,0 | mA   |
| Propagation times            | $T_{amb} = 25^{\circ}C^*$<br>test conditions as in Sub-group A5         | 5,0V           |                   |      |       |      |
| High to Low level            | From                                                                    | To             |                   |      |       |      |
|                              | D                                                                       | $\overline{Q}$ | $t_{PHL}$         | -    | 17,0  | ns   |
|                              | D                                                                       | $\overline{Q}$ | $t_{PHL}$         | -    | 15,0  | ns   |
|                              | G                                                                       | $\overline{Q}$ | $t_{PHL}$         | -    | 25,0  | ns   |
| Low to High level            | From                                                                    | To             |                   |      |       |      |
|                              | D                                                                       | $\overline{Q}$ | $t_{PLH}$         | -    | 27,0  | ns   |
|                              | D                                                                       | $\overline{Q}$ | $t_{PLH}$         | -    | 20,0  | ns   |
|                              | G                                                                       | $\overline{Q}$ | $t_{PLH}$         | -    | 27,0  | ns   |
| Set-up time                  | From                                                                    | To             |                   |      |       |      |
|                              | D                                                                       | $\overline{Q}$ | $t_{PLH}$         | -    | 30,0  | ns   |
|                              | G                                                                       | $\overline{Q}$ | $t_{PLH}$         | -    | 30,0  | ns   |
|                              | G                                                                       | $\overline{Q}$ | $t_{PLH}$         | -    | 30,0  | ns   |
| Set-up time                  |                                                                         |                | $t_{set-up}$      | 20,0 | -     | ns   |
| Duration of Enable pulse     |                                                                         |                | $t_p$<br>(enable) | 20,0 | -     | ns   |
| Hold time                    |                                                                         |                | $t_{hold}$        | 5,0  | -     | ns   |

- (1) Fan out = 10, (2) Fan out = 20,  
(3) Only one output at a time, duration  $t \leq 1$  sec  
\*See 3.2.1 of this specification