

# BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS



Specification available from:- AS SHOWN IN PD 9002  
AND CECC 00 200 AND

BS CECC 90103 - 036

ISSUE 1

AUGUST 1981



Page 1 of 20 pages

## ELECTRONIC COMPONENTS OF ASSESSED QUALITY

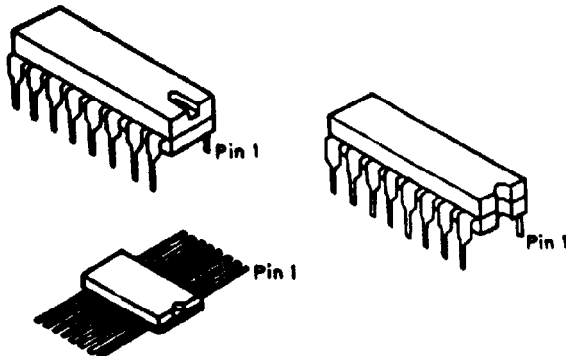
DETAIL SPECIFICATION IN ACCORDANCE WITH:

BS CECC 90 000 : 1976  
BS CECC 90 100 : 1977

## MANUFACTURERS TYPE NUMBER

54LS76A  
64LS76A  
74LS76A  
84LS76A

Outline not to scale: Isometric projection  
Marking information see clause 1



SEE PD 9002 AND CECC 00 200  
For ordering information see  
clause 1

DUAL J-K BISTABLE CIRCUITS  
WITH PRESET AND CLEAR

TYPICAL CONSTRUCTION  
SILICON MONOLITHIC  
BIPOLAR TTL-LOW-POWER  
SCHOTTKY

Refer to IEC 191-1-50a (type A50C)  
Dual-in-Line (plastic or ceramic)  
refer to Appendix A1.3  
Flatpack (metal or ceramic)

ASSESSMENT LEVELS  
R, S, T AND V

### 1. Type description

#### 1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200  
for details of manufacturers approved to this specification

1.1 Truth table (contd)  
(each bistable)

| INPUTS |       |       |   |   | OUTPUTS |             |
|--------|-------|-------|---|---|---------|-------------|
| PRESET | CLEAR | CLOCK | J | K | Q       | $\bar{Q}$   |
| L      | H     | X     | X | X | H       | L           |
| H      | L     | X     | X | X | L       | H           |
| L      | L     | X     | X | X | H*      | $\bar{H}^*$ |
| H      | H     | ↓     | L | L | $Q_0$   | $\bar{Q}_0$ |
| H      | H     | ↓     | H | L | H       | L           |
| H      | H     | ↓     | L | H | L       | H           |
| H      | H     | ↓     | H | H | TOGGLE  |             |
| H      | H     | H     | X | X | $Q_0$   | $\bar{Q}_0$ |

H = High level

L = Low level

X = Logic level irrelevant

$Q_0, \bar{Q}_0$  = The level of Q and  $\bar{Q}$  before the indicated steady level input conditions are established

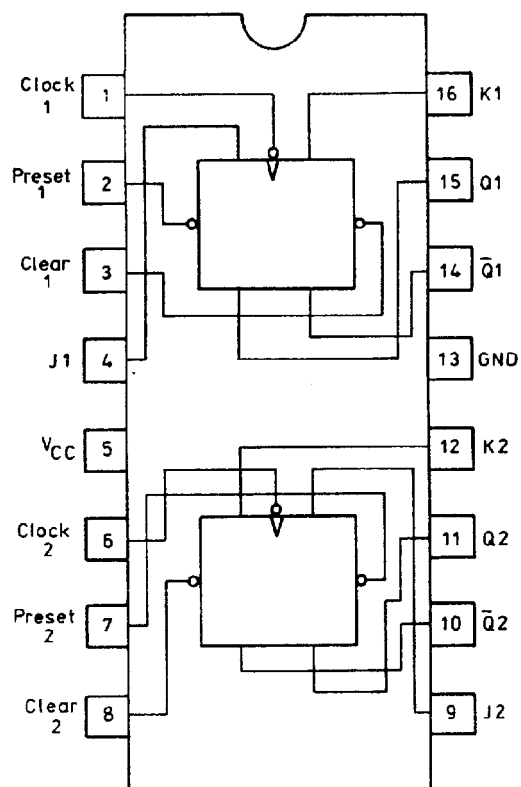
↓ = Clock transition from High to Low level

\* = This condition is unstable and will not persist when preset and clear inputs return to their inactive (High) level

TOGGLE = Each output changes to the complement of its previous level on each ↓ transition of the clock pulse

1.2 Terminal identification, type designation and marking

## 1.2.1 Terminal identification



Dual J-K bistable circuits with preset and clear

## 1.2.2 Type designation

| TEMPERATURE RANGE | PACKAGE              |                      |                  |
|-------------------|----------------------|----------------------|------------------|
|                   | Ceramic Dual-in-Line | Plastic Dual-in-Line | Ceramic Flatpack |
| 0 + 70            | 74LS76AJ             | N                    | W                |
| -25 + 85          | 84LS76AJ             |                      |                  |
| -40 + 85          | 64LS76AJ             |                      |                  |
| -55 +125          | 54LS76AJ             |                      |                  |

### 1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

### 1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

## 2. Limiting conditions of use (not for inspection purposes)

|     |                                   |          |                |
|-----|-----------------------------------|----------|----------------|
| 2.1 | Maximum continuous supply voltage | $V_{CC}$ | -0,5V<br>+7,0V |
|-----|-----------------------------------|----------|----------------|

2.2 Maximum input voltages

|       |                       |       |                |
|-------|-----------------------|-------|----------------|
| 2.2.1 | Maximum input voltage | $V_I$ | -0,5V<br>+7,0V |
|-------|-----------------------|-------|----------------|

|       |                                                                  |          |       |
|-------|------------------------------------------------------------------|----------|-------|
| 2.2.2 | Maximum input voltage between multiple emitter transistor inputs | $V_{II}$ | +5,5V |
|-------|------------------------------------------------------------------|----------|-------|

|     |                                                    |                      | 54LS                  | 64LS        | 74LS     | 84LS       |
|-----|----------------------------------------------------|----------------------|-----------------------|-------------|----------|------------|
| 2.3 | Minimum and maximum operating ambient temperatures | $T_{amb}(^{\circ}C)$ | min. -55<br>max. +125 | -40<br>+85  | 0<br>+70 | -25<br>+85 |
| 2.4 | Minimum and maximum storage temperatures           | $T_{stg}(^{\circ}C)$ | min. -65<br>max. +150 | (All types) |          |            |

## 3. Recommended operating conditions and associated characteristics (not for inspection purposes)

### 3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated

### 3.1 (contd)

| Description                                                                                        | Symbol               | Type                   | Value                    | Unit     |
|----------------------------------------------------------------------------------------------------|----------------------|------------------------|--------------------------|----------|
| Positive supply voltage range                                                                      | $V_{CC}$             | 54LS<br>64/74/84LS     | 4,5 - 5,5<br>4,75 - 5,25 | V<br>V   |
| Minimum value of High level input voltage                                                          | $V_{IHB}$            | All types              | 2,0                      | V        |
| Maximum value of High level input voltage                                                          | $V_{IHA}$            | All types              | 5,5                      | V        |
| Minimum value of Low level input voltage                                                           | $V_{ILB}$            | All types              | -0,3                     | V        |
| Maximum value of Low level input voltage                                                           | $V_{ILA}$            | 54LS<br>64/74/84LS     | 0,7<br>0,8               | V<br>V   |
| Maximum value of Low level output current for each output                                          | $I_{OLA}$            | 54LS<br>64/74/84LS     | 4,0<br>8,0               | mA<br>mA |
| Maximum value of output current for each output at $V_{OH}$                                        | $I_{OHA}$            | All types              | -400,0                   | $\mu$ A  |
| D.C. noise margin<br>at Low level ( $V_{ILA} - V_{OLA}$ )<br>at High level ( $V_{OHB} - V_{IHB}$ ) | $V_{NL}$<br>$V_{NH}$ | All types<br>All types | 0,3<br>0,7               | V<br>V   |

### 3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (\*)

|                       | 54LS | 64LS | 74LS | 84LS |    |
|-----------------------|------|------|------|------|----|
| T <sub>amb</sub> min. | -55  | -40  | 0    | -25  | °C |
| T <sub>amb</sub> max. | +125 | +85  | +70  | +85  |    |
| V <sub>CC</sub> min.  | 4,5  | 4,75 |      |      | V  |
| V <sub>CC</sub> max.  | 5,5  | 5,25 |      |      |    |

3.2.2

| Characteristics                  | Conditions                                                         | $V_{CC}(V)$   | Symbol      | Min. | Max.  | Unit    |
|----------------------------------|--------------------------------------------------------------------|---------------|-------------|------|-------|---------|
| Total supply current per package | All outputs open circuit.<br>Inputs grounded                       | $V_{CC}$ max. | $I_{CC}$    | -    | 8,0   | mA      |
| High level input current         | $V_{IH(1)} = 7,0V$<br>J and K                                      | $V_{CC}$ max. | $I_{IH(1)}$ | -    | 0,1   | mA      |
|                                  | Clear                                                              |               | $I_{IH(1)}$ | -    | 0,3   | mA      |
|                                  | Preset                                                             |               | $I_{IH(1)}$ | -    | 0,3   | mA      |
|                                  | Clock                                                              |               | $I_{IH(1)}$ | -    | 0,4   | mA      |
|                                  | $V_{IH(2)} = 2,7V$<br>J and K                                      |               | $I_{IH(2)}$ | -    | 20,0  | $\mu A$ |
|                                  | Clear                                                              |               | $I_{IH(2)}$ | -    | 60,0  | $\mu A$ |
|                                  | Preset                                                             |               | $I_{IH(2)}$ | -    | 60,0  | $\mu A$ |
|                                  | Clock                                                              |               | $I_{IH(2)}$ | -    | 80,0  | $\mu A$ |
| Low level input current          | $V_{IN} = 0,4V$<br>J and K                                         | $V_{CC}$ max. | $-I_{IL}$   | -    | 0,4   | mA      |
|                                  | Clear                                                              |               | $-I_{IL}$   | -    | 0,8   | mA      |
|                                  | Preset                                                             |               | $-I_{IL}$   | -    | 0,8   | mA      |
|                                  | Clock                                                              |               | $-I_{IL}$   | -    | 0,8   | mA      |
| Input clamping voltage           | $-I_{IC} = 18,0mA$                                                 | $V_{CC}$ min. | $-V_{ICA}$  | -    | 1,5   | V       |
| Output voltage                   | 54LS $I_{OH} = -400,0\mu A$                                        | $V_{CC}$ min. | $V_{OH}$    | 2,5  | -     | V       |
|                                  | 64/74/84LS $I_{OH} = -400,0\mu A$                                  |               | $V_{OH}$    | 2,7  | -     | V       |
|                                  | All types $I_{OL(1)} = 4,0mA$ (1)                                  |               | $V_{OL(1)}$ | -    | 0,4   | V       |
|                                  | 64/74/84LS $I_{OL(2)} = 8,0mA$ (2)                                 |               | $V_{OL(2)}$ | -    | 0,5   | V       |
| Output short circuit current     | $V_{IN} = 0V$ or 4,5V<br>as appropriate<br>$V_O = 0V$ (3)          | $V_{CC}$ max. | $-I_{OS}$   | 15,0 | 130,0 | mA      |
| Propagation times<br>All types   | $T_{amb} = 25^{\circ}C$ *<br>test conditions as<br>in Sub-group A5 | 5,0V          |             |      |       |         |

(1) Fan out = 10, (2) Fan out = 20  
 (3) Only one output at a time, duration  $t \leq 1$  sec  
 \*See 3.2.1 of this specification

## 3.2.2 (contd)

| Characteristics          | Conditions                                          | $V_{CC}(V)$ | Symbol            | Min. | Max. | Unit |
|--------------------------|-----------------------------------------------------|-------------|-------------------|------|------|------|
|                          | <u>From</u> Clear, Preset or Clock (as appropriate) |             | $t_{PHL}$         | -    | 20,0 | ns   |
|                          | <u>To</u> Q or $\bar{Q}$                            |             |                   |      |      |      |
|                          | <u>From</u> Clear, Preset or Clock (as appropriate) |             | $t_{PLH}$         | -    | 20,0 | ns   |
|                          | <u>To</u> Q or $\bar{Q}$                            |             |                   |      |      |      |
| Maximum clock frequency  |                                                     |             | $f_{(clock)}$     | 30,0 | -    | MHz  |
| Duration of clock pulse  |                                                     |             | $t_{p(clock)}$    | 20,0 | -    | ns   |
| Duration of preset pulse |                                                     |             | $t_p$<br>(preset) | 25,0 | -    | ns   |
| Duration of clear pulse  |                                                     |             | $t_{p(clear)}$    | 25,0 | -    | ns   |
| Minimum set-up time      |                                                     |             | $t_{set-up}$      |      |      |      |
| High level data          |                                                     |             |                   | 20,0 | -    | ns   |
| Low level data           |                                                     |             |                   | 20,0 | -    | ns   |
| Hold time                |                                                     |             | $t_{hold}$        | 0    | -    | ns   |

## 3.3 Supplementary information