

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

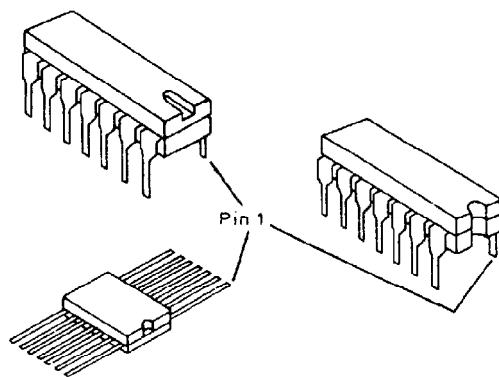
BS CECC 90103 - 041

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**ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:**BS CECC 90 000 : 1976
BS CECC 90 100 : 1977**MANUFACTURERS TYPE NUMBER**54LS90
64LS90
74LS90
84LS90Outline not to scale: Isometric projection
Marking information see clause 1Refer to IEC 191-1-50a (type A50B)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1DECADE DIVIDE-BY-TWO AND
DIVIDE-BY-FIVE COUNTERS,
SUPPLY TO PINS 5 AND 10TYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR TTL-LOW-POWER
SCHOTTKYASSESSMENT LEVELS
R, S, T AND V1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Output Q_A is connected to input B for BCD count

BI-QUINARY (5-2)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

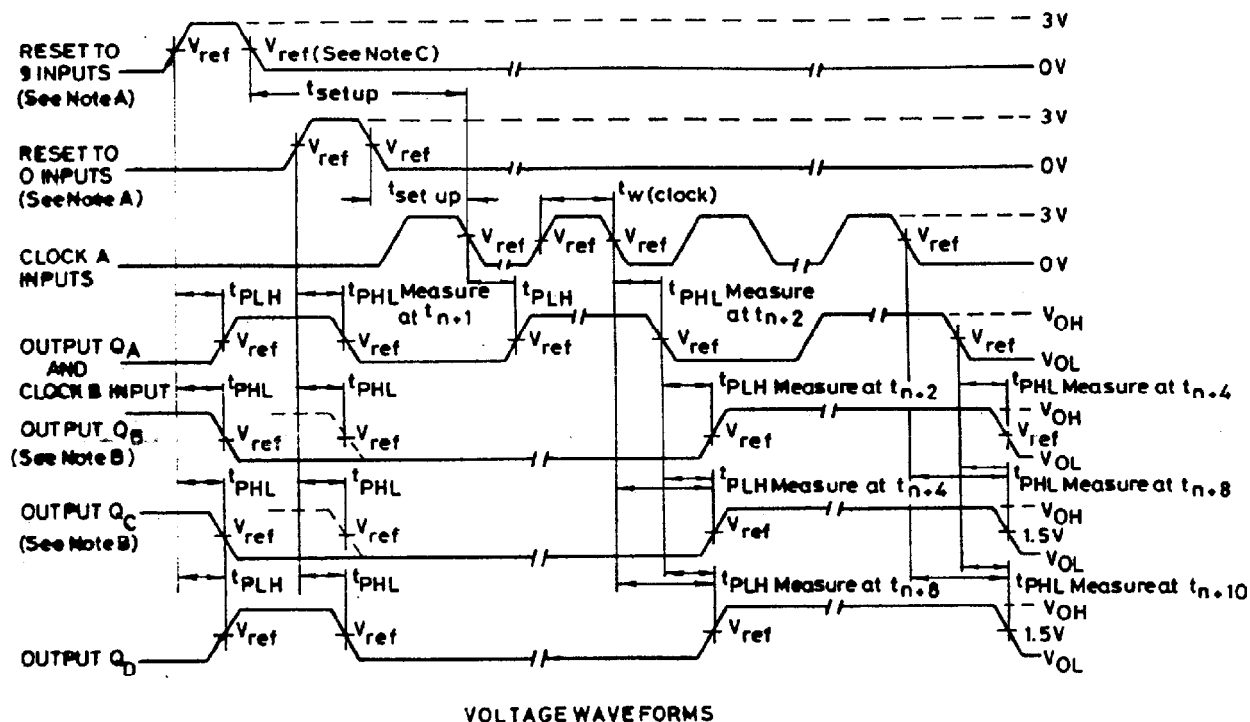
Output Q_D is connected to input A for bi-quinary count

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R _O (1)	R _O (2)	R _g (1)	R _g (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L		COUNT		
L	X	L	X				
L	X	X	L				
X	L	L	X				

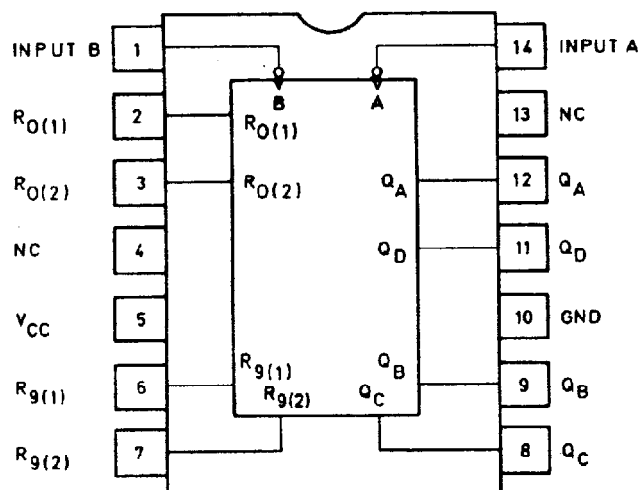
H = High level
L = Low level
X = Logic level irrelevant

1.1.1 Typical operating waveform diagram



1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Decade divide-by-two and divide-by-five counters, supply to pins 5 and 10

Terminals marked with 'NC' are not connected internally and may be used as electrical support points. The applied voltage shall not exceed 7,0V.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS90J	N	W
-25 + 85	84LS90J		
-40 + 85	64LS90J		
-55 +125	54LS90J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
				54LS	64LS	74LS	84LS	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	-55	-40	0	-25	
			max.	+125	+85	+70	+85	

2.4 Minimum and maximum storage temperatures $T_{stg}(^{\circ}C)$ min. -65 max. +150 (All types)

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range, unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage, Reset inputs A and B inputs	V_{IHB}	All types	2,0 2,0	V V
Maximum value of High level input voltage, Reset inputs A and B inputs	V_{IHA}	All types	5,5 5,5	V V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IL} = 0V$ (1)	$V_{CC} \text{ max.}$	I_{CC}	-	15,0	mA
High level input current	$V_{IH(1)} = 7,0V$ $V_{IH(2)} = 2,7V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,1	mA
Reset inputs			$I_{IH(1)}$	-	0,2	mA
A input			$I_{IH(1)}$	-	0,4	mA
B input			$I_{IH(2)}$	-	20,0	μA
Reset inputs			$I_{IH(2)}$	-	40,0	μA
A input			$I_{IH(2)}$	-	80,0	μA
B input						
Low level input current						
Reset inputs						
A input	$V_{IL} = 0,4V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
B input			$-I_{IL}$	-	2,4	mA
			$-I_{IL}$	-	3,2	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage	54LS $I_{OH} = -400,0\mu A$ 64/74/84LS $I_{OH} = -400,0\mu A$ All types $I_{OL(1)} = 4,0mA$ (2) 64/74/84LS $I_{OL(2)} = 8,0mA$ (3)	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
			V_{OH}	2,7	-	V
			$V_{OL(1)}$	-	0,4	V
			$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ (4)	$V_{CC} \text{ max.}$	$-I_{OS}$	20,0	130,0	mA
Propagation times	$T_{amb} = 25^\circ C^*$ Test conditions as Sub-group A5	5,0V	t_{PHLA}			
All types						
High to Low level						
From	To					
A	Q_A					
A	Q_D					
B	Q_B					
B	Q_C					
B	Q_D					
Set-to-0	Any					
Set-to-9	Q_B, Q_C					

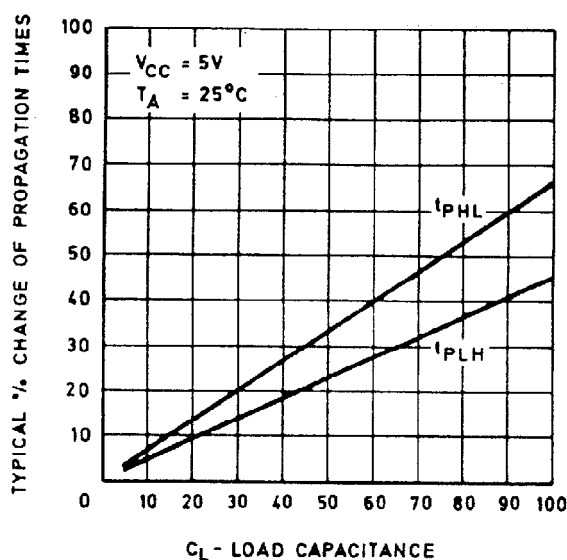
- (1) To all inputs, (2) Fan out = 10, (3) Fan out = 20,
 (4) Only one output at a time, duration $t \leq 1 \text{ sec}$
 * See 3.2.1 of this specification

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Low to High level			t_{PLHA}			
From A To Q_A				-	16,0	ns
A Q_D				-	48,0	ns
B Q_B				-	16,0	ns
B Q_C				-	32,0	ns
B Q_D				-	32,0	ns
Set-to-9 Q_A, Q_D				-	30,0	ns
Reset inactive-level set up time			t_{set-up}	25,0	-	ns
Input pulse width						
From A			t_p	15,0	-	ns
B			t_p	30,0	-	ns
Reset			t_p	15,0	-	ns
Switching Frequency						
A			$F_{max.}$	32,0	-	MHz
B			$F_{max.}$	16,0	-	MHz

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation time Vs. load capacitance