

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90103 - 042

ISSUE 1

NOVEMBER 1981



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ELECTRONIC COMPONENTS OF ASSESSED QUALITY

DETAIL SPECIFICATION IN ACCORDANCE WITH:

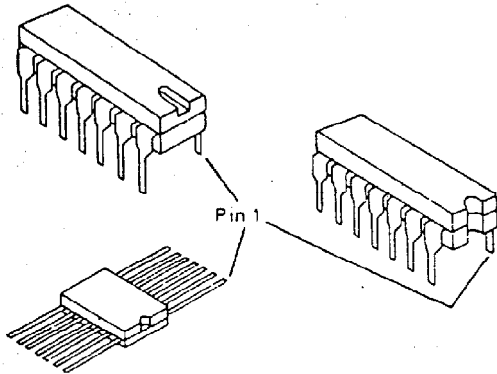
BS CECC 90 000 : 1976
BS CECC 90 100 : 1977**MANUFACTURERS TYPE NUMBER**

54LS91

64LS91

74LS91

84LS91

Outline not to scale: Isometric projection
Marking information see clause 1Refer to IEC 191-1-50a (type A50B)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)SEE PD 9002 AND CECC 00 200
For ordering information see
clause 18-BIT SERIAL-IN SERIAL-OUT
SHIFT REGISTERS WITH GATED
INPUTSTYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR TTL-LOW-POWER
SCHOTTKYASSESSMENT LEVELS
R, S, T AND V1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification**Documents**

Document Sharing Hub

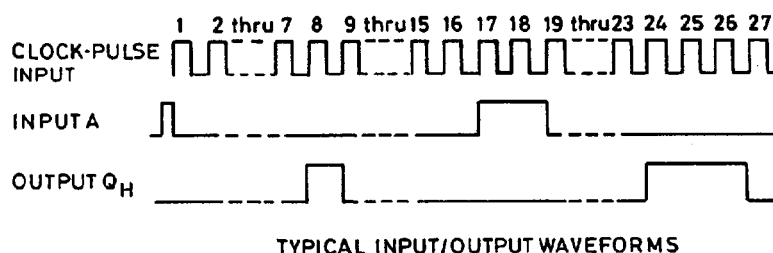
1.1 Truth table (contd)

INPUTS at t_n		OUTPUTS at $t_n + 8$	
A	B	Q_H	$\overline{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

H = High level
 L = Low level
 X = Logic level irrelevant
 t_n = Reference bit time, clock Low
 $t_n + 8$ = Bit time after 8 Low to High clock transitions

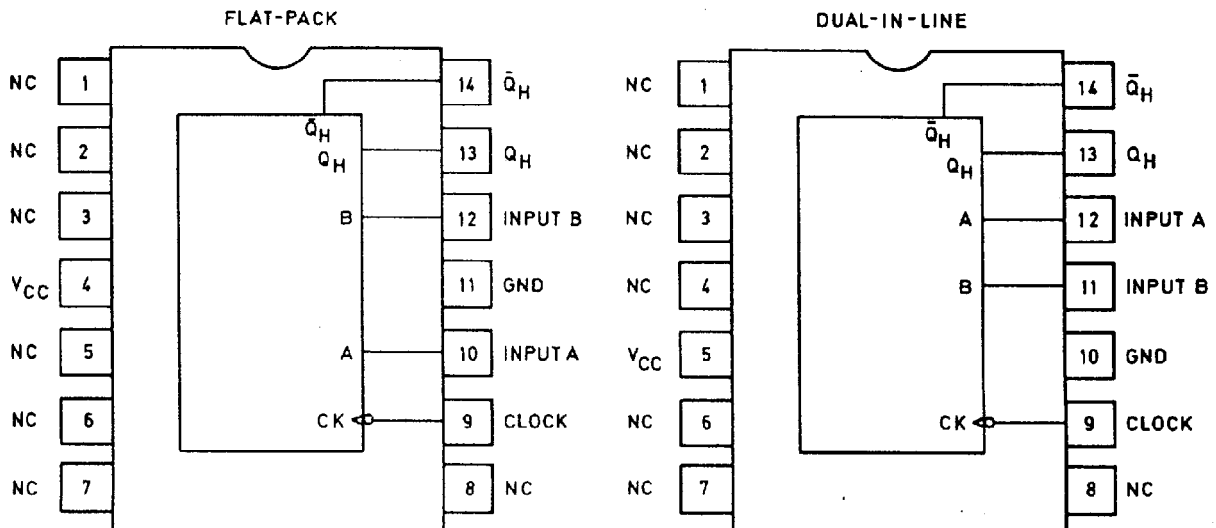
These monolithic serial-in, serial-out 8-bit shift registers are composed of eight R-S master-slave bistables, input gating and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

1.1.1 Typical operating waveform



1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



8-bit serial-in serial-out shift
registers with gated inputs

Terminals marked with 'NC' are not connected internally and may be used as electrical support points. The applied voltage shall not exceed 7,0V.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS91J	N	W
-25 + 85	84LS91J		
-40 + 85	64LS91J		
-55 +125	54LS91J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
				54LS	64LS	74LS	84LS	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	-55	-40	0	-25	
			max.	+125	+85	+70	+85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)			
			max.	+150				

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

3.1 (contd)

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μ A

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IL} = 0V$ (1)	$V_{CC} \text{ max.}$	I_{CC}	-	20,0	mA
High level input current	$V_{IH(1)} = 7,0V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	100,0	μA
	$V_{IH(2)} = 2,7V$		$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	mA
Output voltage	54LS $I_{OH} = -400,0\mu A$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
	64/74/84LS $I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
	All types $I_{OL(1)} = 4,0mA$ (2)		$V_{OL(1)}$	-	0,4	V
	64/74/84LS $I_{OL(2)} = 8,0mA$ (3)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ or $4,5V$ (4) $V_{IL} = 0V$	$V_{CC} \text{ max.}$	$-I_{OS}$	20,0	100,0	mA
Propagation times	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V	t_{PLH}	-	40,0	ns
			t_{PHL}	-	40,0	ns
Duration of Clock pulse			$t_{p(\text{clock})}$	25,0	-	ns
Set-up time			$t_{(\text{set-up})}$	25,0	-	ns
Hold time			$t_{(\text{hold})}$	0	-	ns
Maximum clock frequency			$f_{\text{max.}}$	10,0	-	MHz

(1) To all inputs, (2) Fan out = 10, (3) Fan out = 20,

(4) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See 3.2.1 of this specification