

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

BS CECC 90103 - 044

ISSUE 1

NOVEMBER 1981



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ELECTRONIC COMPONENTS OF ASSESSED QUALITY**DETAIL SPECIFICATION IN ACCORDANCE WITH:**

BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

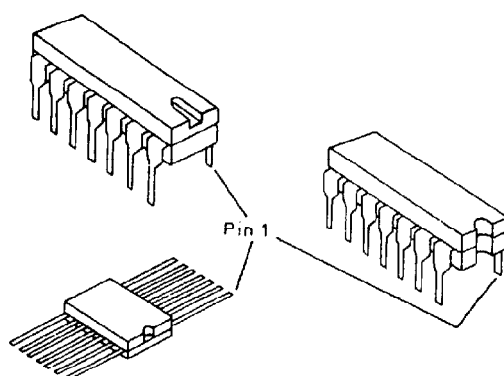
54LS93

64LS93

74LS93

84LS93

Outline not to scale: Isometric projection
Marking information see clause 1



Refer to IEC 191-1-50a (type A50B)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)

SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1

4-BIT BINARY COUNTER

TYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR TTL-LOW-POWER
SCHOTTKY

ASSESSMENT LEVELS
R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

Count Sequence:

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Reset/Count Function Table

RESET INPUTS		OUTPUT			
R _O (1)	R _O (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT COUNT	COUNT COUNT	L	L
X	L				

NOTE: Output Q_A is connected to input B

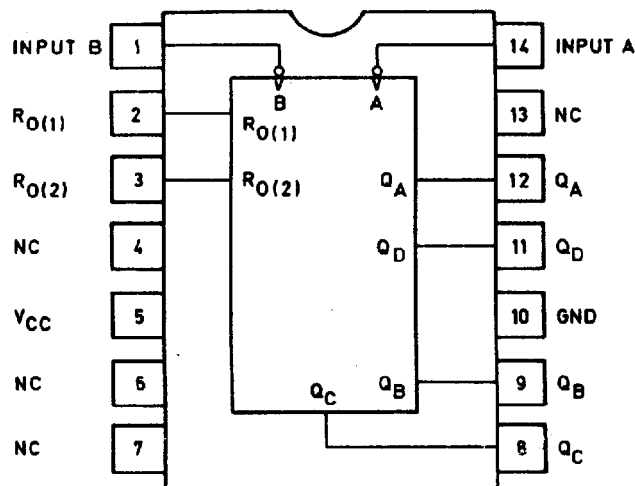
H = High level

L = Low level

X = Logic level irrelevant

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



4-bit binary counters

Terminals marked 'NC' are not connected internally and may be used as electrical support points. The applied voltage shall not exceed 7,0V.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS93J	N	W
-25 + 85	84LS93J		
-40 + 85	64LS93J		
-55 +125	54LS93J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection puposes)

2.1	Maximum continuous supply voltage	V_{CC}		-0,5V +7,0V
2.2	Maximum input voltages			
2.2.1	Maximum input voltage	V_I		-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}		+5,5V
			54LS 64LS 74LS 84LS	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85 0 +70 -25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IL} = 0V$ (1)	V_{CC} max.	I_{CC}	-	15,0	mA
High level input current Any Reset A input B input Any Reset A input B input	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
	$V_{IH(1)} = 5,5V$			-	0,2	mA
	$V_{IH(1)} = 5,5V$			-	0,4	mA
	$V_{IH(2)} = 2,7V$		$I_{IH(2)}$	-	20,0	µA
				-	40,0	µA
				-	80,0	µA
Low level input current Any Reset A input B input	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
				-	2,4	mA
				-	1,6	mA
				-	1,6	mA
input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage 54LS 64/74/84LS All types 64/74/84LS	$I_{OH} = -400,0\mu A$	V_{CC} min.	V_{OH}	2,5	-	V
	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
	$I_{OL(1)} = 4,0mA$ (2)		$V_{OL(1)}$	-	0,4	V
	$I_{OL(2)} = 8,0mA$ (3)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ (4) $V_{IL} = 0V$	V_{CC} max.	$-I_{OS}$	15,0	130,0	mA

- (1) To all inputs, (2) Fan out = 10, (3) Fan out = 20,
(4) Only one output at a time, duration $t \leq 1$ sec

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Propagation times All types	$T_{amb} = 25^{\circ}C^{*}$ test conditions as in Sub-group A5	5,0V				
From To						
A Q_A			t_{PHL}	-	18,0	ns
A Q_D				-	70,0	ns
B Q_B				-	21,0	ns
B Q_C				-	35,0	ns
B Q_D				-	51,0	ns
Set-to-0 Any				-	40,0	ns
From To						
A Q_A			t_{PLH}	-	16,0	ns
A Q_D				-	70,0	ns
B Q_B				-	16,0	ns
B Q_C				-	32,0	ns
B Q_D				-	51,0	ns
Maximum clock frequency	A input B input		$f_{(clock)}$	32,0 16,0	- -	MHz MHz
Duration of clock pulse	A input B input		$t_{p(clock)}$	15,0 30,0	- -	ns ns
Duration of reset pulse	Reset input		$t_{p(reset)}$	15,0	-	ns
Set-up time			t_{set-up}	25,0	-	ns

* See 3.2.1 of this specification