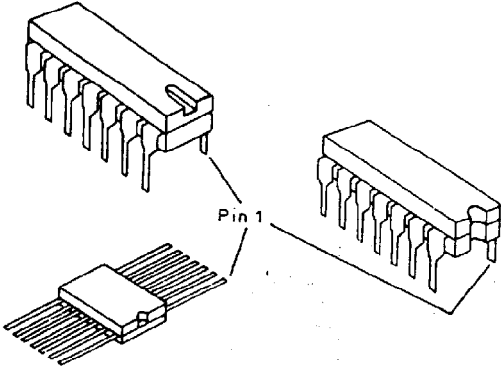


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	BS CECC 90103 - 046 ISSUE 1 JULY 1981  Page 1 of 17 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS107A 64LS107A 74LS107A 84LS107A
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50B) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 DUAL J-K MASTER-SLAVE BISTABLE WITH CLEAR TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

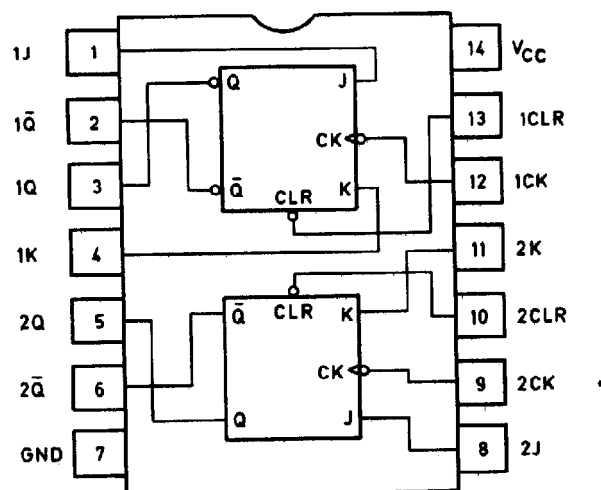
1.1 Truth table (each bistable)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	Q_0	$\bar{Q}_0$

H = High level
 L = Low level
 ↓ = Transition from High to Low level
 X = Logic level irrelevant
 Q_0 = Level of Q before the indicated steady level conditions were established

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Dual J-K master-slave bistable with clear

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS107J	N	W
-25 + 85	84LS107J		
-40 + 85	64LS107J		
-55 +125	54LS107J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}					-0,5V +7,0V
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I					-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}					+5,5V
2.3	Maximum and minimum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	54LS -55 +125	64LS -40 +85	74LS 0 +70	84LS -25 +85
2.4	Maximum and minimum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T_{amb} min.	-55	-40	0	-25	$^{\circ}C$
T_{amb} max.	+125	+85	+70	+85	
V_{CC} min.	4,5	4,75			V
V_{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IL} = 0V$ (1)	V_{CC} max.	I_{CC}	-	6,0	mA
High level input current J and K inputs	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
Clear input				-	0,3	mA
Clock input				-	0,4	mA
J and K inputs	$V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(2)}$	-	20,0	μA
Clear input				-	60,0	μA
Clock input				-	80,0	μA
Low level input current J and K inputs	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
Clear input				-	0,8	mA
Clock input				-	0,8	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage 54LS	$I_{OH} = -400,0\mu A$	V_{CC} min.	V_{OH}	2,5	-	V
64/74/84LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
All types	$I_{OL(1)} = 4,0mA$ (2)		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA$ (3)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ (4) $V_{IL} = 0V$	V_{CC} max.	$-I_{OS}$	15,0	130,0	mA
Propagation times	$T_{amb} = 25^\circ C^*$	5,0V				
All types	test conditions as in Sub-group A5		t_{PHL}	-	20,0	ns
			t_{PLH}	-	20,0	ns
Duration of clock pulse (Clock High) (Clear Low)			$t_{p(clock)}$	20,0 25,0	- -	ns ns
Minimum set-up time with respect to negative edge of clock			$t_{(set-up)}$	20,0 $\downarrow$	-	ns
Maximum clock frequency			$f_{(clock)}$	30,0	-	MHz
Minimum hold time with respect to negative edge of clock			$t_{(hold)}$	0 $\downarrow$	-	-

$\downarrow$ = With respect to the falling edge of the clock pulse

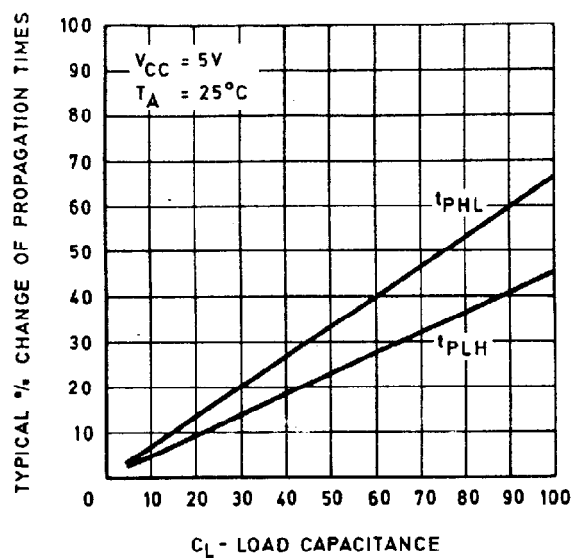
(1) To all inputs, (2) Fan out = 10, (3) Fan out = 20,

(4) Only one output at a time duration $t \leq 1$ sec

*See 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance

3.3.2 Variation of propagation time with temperature

