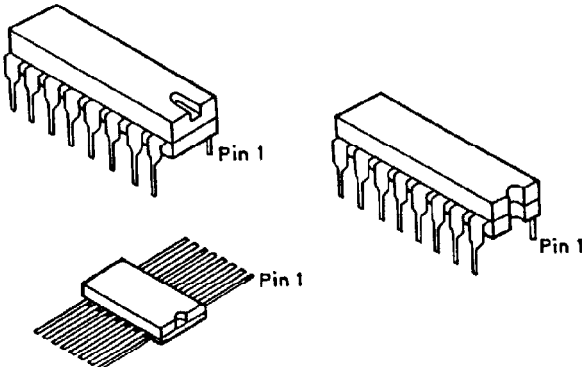


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	BS CECC 90103 - 047 ISSUE 1 NOVEMBER 1981 Page 1 of 18 pages 
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS109A 64LS109A 74LS109A 84LS109A
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 DUAL J-K POSITIVE EDGE TRIGGERED BISTABLE WITH PRESET, CLEAR TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\bar{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\bar{Q}_0$

H = High level (steady level)

L = Low level (steady level)

X = Logic level irrelevant

↑ = Transition from Low to High level

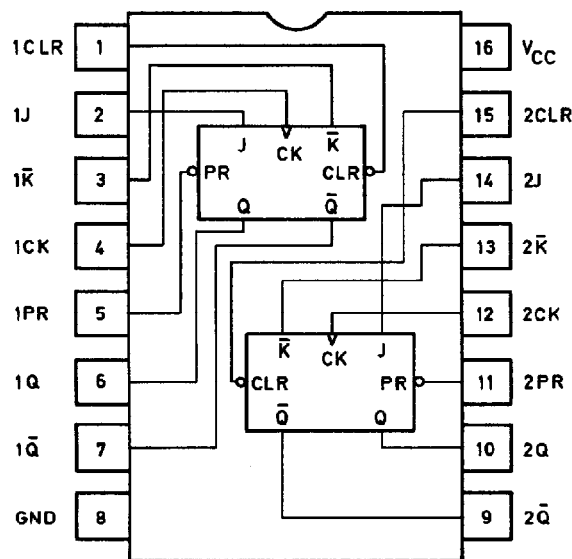
Q_0 = The level of Q before the indicated input conditions were established

TOGGLE = Each output changes to the complement of its previous level on each active transition of the clock

* = This configuration is non-stable, that is, it will not persist when preset and clear inputs return to their inactive (High) level

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Dual J-K positive edge triggered bistable with preset, clear

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS109AJ	N	W
-25 + 85	84LS109AJ		
-40 + 85	64LS109AJ		
-55 +125	54LS109AJ		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection puposes)

2.1 Maximum continuous supply voltage V_{CC} -0,5V
+7,0V

2.2 Maximum input voltages

2.2.1 Maximum input voltage V_I -0,5V
+7,0V

2.2.2 Maximum input voltage between multiple emitter transistor inputs V_{II} +5,5V

			54LS	64LS	74LS	84LS
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85	0 +70	-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μ A

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IL} = 0V$ (1)	$V_{CC} \text{ max.}$	I_{CC}	-	8,0	mA
High level input currents:	$V_{IH(1)} = 7,0V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,1	mA
J or $\bar{K}$				-	0,2	mA
Clear				-	0,2	mA
Preset				-	0,1	mA
Clock				-	20,0	μA
J or $\bar{K}$			$I_{IH(2)}$	-	40,0	μA
Clear				-	40,0	μA
Preset				-	20,0	μA
Clock				-		
Low level input current	$V_{IL} = 0,4V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
J or $\bar{K}$				-	0,8	mA
Clear				-	0,8	mA
Preset				-	0,4	mA
Clock				-		
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage 54LS	$I_{OH} = -400,0\mu A$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
64/74/84LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
All types	$I_{OL(1)} = 4,0mA$ (2)		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA$ (3)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ (4)	$V_{CC} \text{ max.}$	$-I_{OS}$	20,0	100,0	mA
Propagation times	$T_{amb} = 25^\circ C^*$	5,0V				
All types	test conditions as in Sub-group A5					
From			t_{PLH}	-	25,0	ns
Clear, preset or clock (as appropriate)						
To			t_{PHL}	-	40,0	ns
Q or $\bar{Q}$						
From						
Clear, preset or clock (as appropriate)						
To						
Q or $\bar{Q}$						

(1) To all inputs, (2) Fan out = 10, (3) Fan out = 20,

(4) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See 3.2.1 of this specification

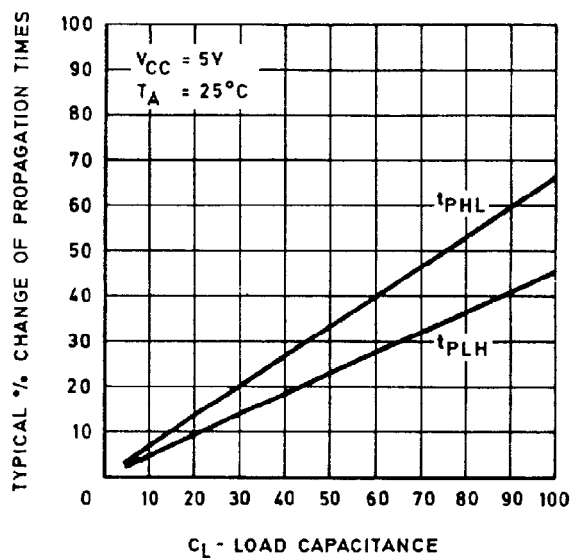
3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Maximum clock frequency			$f_{(clock)}$	25,0	-	ns
Duration of clock pulse			$t_{p(clock)}$	25,0	-	ns
Duration of preset pulse			$t_{p(preset)}$	25,0	-	ns
Duration of clear pulse			$t_{p(clear)}$	25,0	-	ns
Minimum hold time			$t_{(hold)}$	5,0†	-	ns
Minimum set-up time			$t_{(set-up)}$			
High level data				20,0†	-	ns
Low level data				20,0†	-	ns

† = The arrow indicates the rising edge of the clock pulse is used for reference

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance