

BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 050 ISSUE 1 NOVEMBER 1981
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	 <

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200 for details of manufacturers approved to this specification

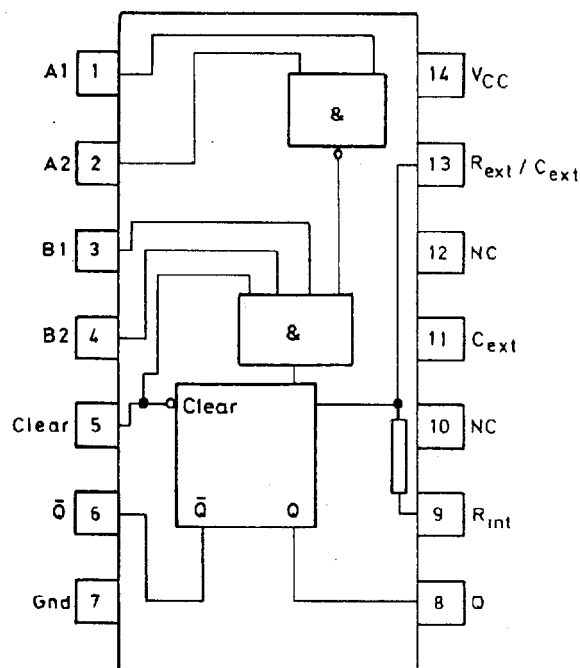
1.1 Truth table (contd)

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⌊	⌋
H	L	X	H	↑	⌊	⌋
H	X	L	H	H	L	H
H	X	L	↑	H	⌊	⌋
H	X	L	H	↑	⌊	⌋
H	H	↓	H	H	⌊	⌋
H	↓	↓	H	H	⌊	⌋
H	↓	H	H	H	⌊	⌋
↑	L	X	H	H	⌊	⌋
↑	X	L	H	H	⌊	⌋

H = High level
 L = Low level
 ↑ = Low to high level transition
 ↓ = High to low level transition
 ⌊ = One high level pulse
 ⌋ = One low level pulse
 X = Logic level irrelevant

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



NC = Not connected

Retriggerable monostable multivibrators with clear

Terminals marked with NC are not connected internally and may be used as electrical support points. The applied voltage shall not exceed 7,0V.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS122J	N	W
-25 + 85	84LS122J		
-40 + 85	64LS122J		
-55 +125	54LS122J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

3.1 (contd)

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2.0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μ A
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V
C. external	C_{ext}	All types	No Limit	
External timing resistor	R_{ext}	54LS 64/74/84LS	5 to 180 5 to 280	k Ω k Ω
Wiring capacitance max. limit			50	pF

3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

3.2.1 (contd)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	With all outputs open and 4,5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4,5V is applied to clock.	V_{CC} max.	I_{CC}	-	11,0	mA
High level input current	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
	$V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IN} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	4,5V	$-V_{IC}$	-	1,5	V
Output voltage 54LS 64/74/84LS All types 64/74/84LS	$V_{IN} = V_{ILA}$ or V_{IHB}	V_{CC} min.				
	To measure V_{OH} at Q		V_{OH}	2,5	-	V
	and V_{OL} at $\bar{Q}$, Ground		V_{OH}	2,7	-	V
	R_{ext}/C_{ext} , apply		$V_{OL(1)}$	-	0,4	V
	2,0V to B and Clear and pulse A from (1)		$V_{OL(2)}$	-	0,5	V

(1) Refer to truth table

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output short circuit current	$V_{IN} = 0V$ or $4,5V$ To measure on I_{OS} at Q, Ground R_{ext}/C_{ext} , apply $2,0V$ to B or Clear and pulse A from $2,0V$ to $10,0V$	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times All types	$T_{amb} = 25^{\circ}C$ test conditions as in Sub-group A5	5,0V				
High to Low level	From To A $\overline{Q}$ B $\overline{Q}$ Clear Q		t_{PHLA} t_{PHLA} t_{PHLA}	- - -	45,0 56,0 27,0	ns ns ns
Low to High level	From To A Q B Q Clear $\overline{Q}$		t_{PLHA} t_{PLHA} t_{PLHA}	- - -	33,0 44,0 45,0	ns ns ns
Input pulse width			t_p	40,0	-	ns
Minimum output Q pulse width	From A or B to Q		t_{pQ}	-	200,0	ms
Output pulse width	$C_{ext} = 1000,0pF$ $R_{ext} = 10,0k\Omega$ From A or B to Q†		t_{pQ}	4,0	5,0	ns

*See 3.2.1 of this specification

†See Appendix A1.3