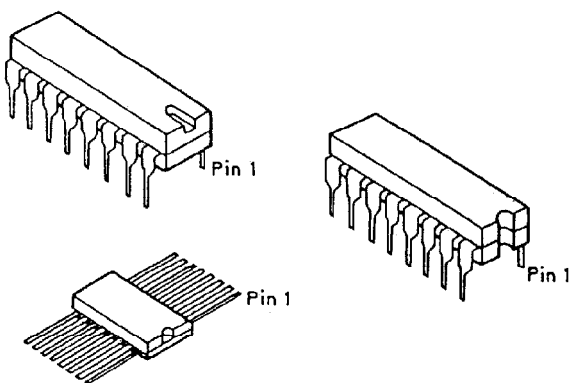




BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 051 ISSUE 1 NOVEMBER 1981 
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	Page 1 of 21 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS123 64LS123 74LS123 84LS123 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	DUAL RETRIGGERABLE MONOSTABLE WITH CLEAR TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description
 - 1.1 Truth table (each multivibrator) (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (each multivibrator) (contd)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⌈	⌋
H	↓	H	⌋	⌈
↑	L	H	⌈	⌋

H = High level
 L = Low level
 X = Logic level irrelevant
 ↑ = Low to High level transition
 ↓ = High to low level transition
 ⌈ = One High level pulse
 ⌋ = One Low level pulse

1.1.1 Timing relationship (see Appendix A1.4)

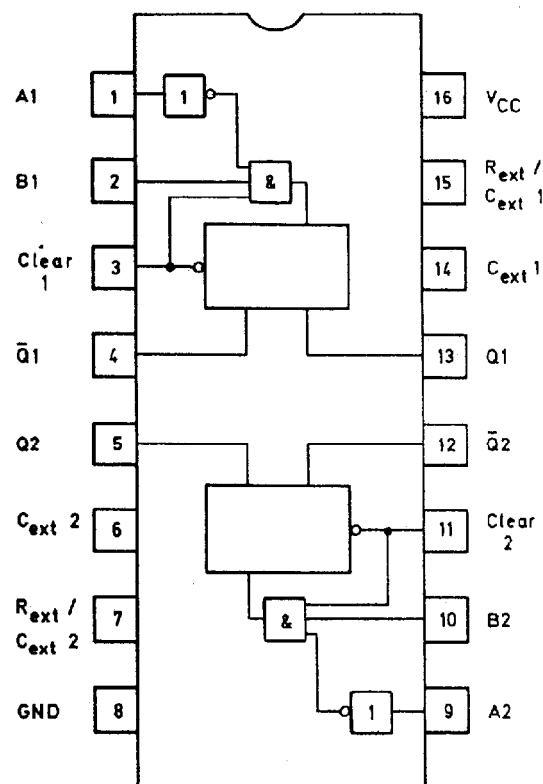
The output pulse width is a function of the external capacitor and resistor when $C_{ext} > 1000\text{pF}$, the output pulse width is defined as follows:

$$t_p = 0,45 \times RT \times C_{ext}$$

RT = internal timing resistor in $k\Omega$
 C_{ext} is in pF
 t_p is in ns

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Dual retriggerable monostable multivibrator with clear

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS123J	N	W
-25 + 85	84LS123J		
-40 + 85	64LS123J		
-55 +125	54LS123J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
				54LS	64LS	74LS	84LS	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	-55	-40	0	-25	
			max.	+125	+85	+70	+85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)			
			max.	+150				

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V

3.1 (contd)

Description	Symbol	Type	Value	Unit
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μ A
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V
C_{ext}		All types	No Limit	
External timing resistor		54LS 64/74/84LS	5 - 180 5 - 280	k Ω k Ω
Wiring capacitance max. limit			50	pF

3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	With all outputs open and 4,5V applied to all Data and Clear input I_{CC} is measured after a momentary Ground, then 4,5V is applied to Clock.	V_{CC} max.	I_{CC}	-	20,0	mA
High level input current	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
	$V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IN} = 0,4V$ applied to each input in turn, other like inputs at 4,5V	V_{CC} max.	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	4,5V	$-V_{ICA}$	-	1,5	V
Output voltage 54LS 64/74/84LS All types 64/74/84LS	$V_{IN} = V_{ILA}$ or V_{IHB}	V_{CC} min.	V_{OH}	2,5	-	V
	To measure V_{OH} at Q and V_{OL} at $\bar{Q}$, Ground R_{ext}/C_{ext} , apply 2,0V to B and Clear and pulse A from 2,0V to 0V (1)		V_{OH}	2,7	-	V
			$V_{OL(1)}$	-	0,4	V
			$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_{IN} = 0V$ or 4,5V To measure on I_{OS} at Q, Ground R_{ext}/C_{ext} , apply 2,0V to B or Clear and pulse A from 2,0V to 0V	V_{CC} max.	$-I_{OS}$	20,0	100,0	mA
Wiring capacitance	At C_{ext}/R_{ext} terminal			-	50,0	pF

(1) Refer to truth table

3.2.2 (contd)

Characteristics	Conditions	V _{CC} (V)	Symbol	Min.	Max.	Unit																				
Propagation times All types	T _{amb} = 25°C* test conditions as in Sub-group A5	5,0V																								
High to Low level	<table><tr><td>From</td><td>To</td></tr><tr><td>A</td><td>$\overline{Q}$</td></tr><tr><td>B</td><td>$\overline{Q}$</td></tr><tr><td>Clear</td><td>Q</td></tr></table>	From	To	A	$\overline{Q}$	B	$\overline{Q}$	Clear	Q		<table><tr><td>t_{PHL}</td><td>-</td><td>45,0</td><td>ns</td></tr><tr><td>t_{PHL}</td><td>-</td><td>56,0</td><td>ns</td></tr><tr><td>t_{PHL}</td><td>-</td><td>27,0</td><td>ns</td></tr></table>	t _{PHL}	-	45,0	ns	t _{PHL}	-	56,0	ns	t _{PHL}	-	27,0	ns			
From	To																									
A	$\overline{Q}$																									
B	$\overline{Q}$																									
Clear	Q																									
t _{PHL}	-	45,0	ns																							
t _{PHL}	-	56,0	ns																							
t _{PHL}	-	27,0	ns																							
Low to High level	<table><tr><td>From</td><td>To</td></tr><tr><td>A</td><td>Q</td></tr><tr><td>B</td><td>Q</td></tr><tr><td>Clear</td><td>$\overline{Q}$</td></tr></table>	From	To	A	Q	B	Q	Clear	$\overline{Q}$		<table><tr><td>t_{PLH}</td><td>-</td><td>33,0</td><td>ns</td></tr><tr><td>t_{PLH}</td><td>-</td><td>44,0</td><td>ns</td></tr><tr><td>t_{PLH}</td><td>-</td><td>45,0</td><td>ns</td></tr></table>	t _{PLH}	-	33,0	ns	t _{PLH}	-	44,0	ns	t _{PLH}	-	45,0	ns			
From	To																									
A	Q																									
B	Q																									
Clear	$\overline{Q}$																									
t _{PLH}	-	33,0	ns																							
t _{PLH}	-	44,0	ns																							
t _{PLH}	-	45,0	ns																							
Input pulse width			t _p	40,0	-	ns																				
Minimum output Q pulse width			t _{pQ}	-	200,0	ns																				
Output pulse width (See Appendix A1.4)	C _{ext} = 100pF R _{ext} = 10kΩ		t _{pQ}	4,0	5,0	ns																				

*See 3.2.1 of this specification

3.3 Supplementary information

