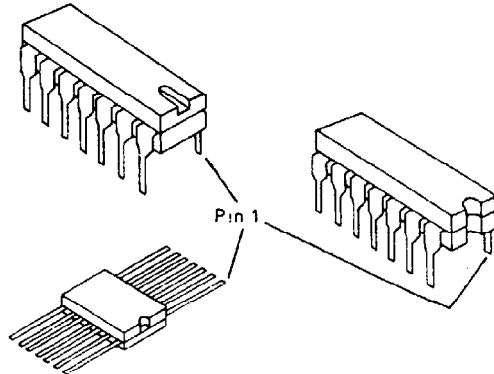


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 054 ISSUE 1 NOVEMBER 1981	
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	Page 1 of 19 pages	
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS126A 64LS126A 74LS126A 84LS126A SEE PD 9002 AND CECC 00 200 For ordering information see clause 1	
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50B) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	QUADRUPLE BUS BUFFER GATES WITH THREE-LEVEL OUTPUTS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY	
	ASSESSMENT LEVELS R, S, T AND V	

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS		OUTPUTS
CONTROL	A	Y
L	X	Z
H	L	L
H	H	H

H = High level

L = Low level

X = Logic level irrelevant

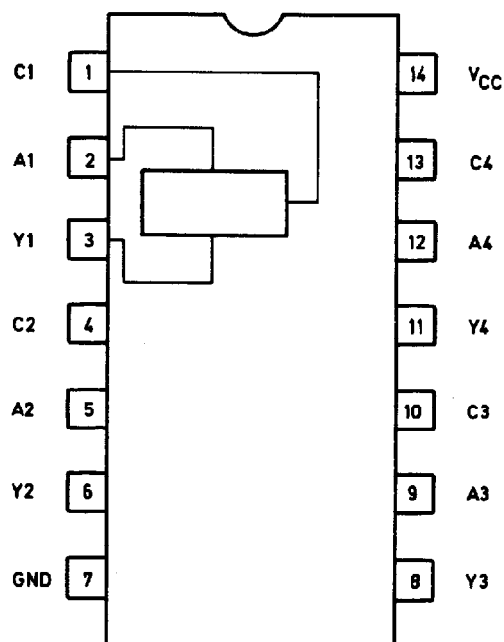
Z = High impedance level (output disabled)

1.1.1 Boolean equation

$$Y = A$$

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Quadruple bus buffer gates with three-level outputs

Three level device

A device whose output can be driven into a High, Low or high impedance level.

High impedance level

That level of a device in which the output acquires a high impedance characteristic.

High impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high impedance level.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS 126AJ	N	W
-25 + 85	84LS 126AJ		
-40 + 85	64LS 126AJ		
-55 +125	54LS 126AJ		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V												
2.2	Maximum input voltages														
2.2.1	Maximum input voltage	V_I	-0,5V +7,0V												
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V												
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	<table> <tr> <td>54LS</td><td>64LS</td><td>74LS</td><td>84LS</td></tr> <tr> <td>min. -55</td><td>-40</td><td>0</td><td>-25</td></tr> <tr> <td>max. +125</td><td>+85</td><td>+70</td><td>+85</td></tr> </table>	54LS	64LS	74LS	84LS	min. -55	-40	0	-25	max. +125	+85	+70	+85
54LS	64LS	74LS	84LS												
min. -55	-40	0	-25												
max. +125	+85	+70	+85												
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	<table> <tr> <td>min. -65</td><td colspan="3">(All types)</td></tr> <tr> <td>max. +150</td><td colspan="3"></td></tr> </table>	min. -65	(All types)			max. +150							
min. -65	(All types)														
max. +150															

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V (
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	12,0 24,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	54LS 64/74/84LS	-1,0 -2,6	mA mA
High impedance level output leakage current	I_{OHZ} $-I_{OLZ}$	All types All types	20,0 20,0	μ A μ A
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V
Maximum applied off-level output voltage	V_{OZA}	All types	5,5	V

3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

3.2.1 (contd)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IL} = 0V$ (1) Outputs open circuit	V_{CC} max.	I_{CC}	-	22,0	mA
High level input current	$V_{IH(1)} = 7,0V$ $V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
		V_{CC} max.	$I_{IH(2)}$	-	20,0	µA
Low level input current	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage	$V_{IN} = V_{ILA}^*$ or 2,0V as appropriate	V_{CC} min.				
			V_{OH}	2,4	-	V
			$V_{OL(1)}$	-	0,4	V
			$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ (4)	V_{CC} max.	$-I_{OS}$	15,0	225,0	mA
Propagation times	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
			t_{PLH}	-	15,0	ns
			t_{PHL}	-	18,0	ns

(1) To all inputs. (2) Fan out = 10, (3) Fan out = 20,

(4) Only one output at a time, duration $t \leq 1$ sec

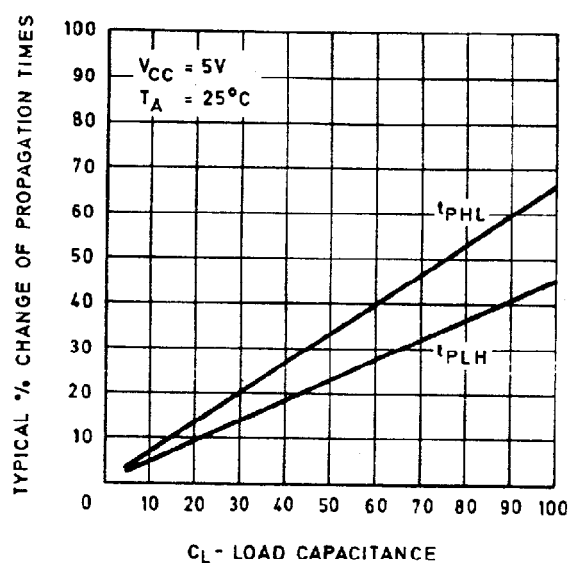
*See 3.2.1 of this specification

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
High impedance to High level (output enable)			t_{PZH}	-	25,0	ns
High impedance to Low level (output enable)			t_{PZL}	-	35,0	ns
High level to high impedance (output disable)	$C_L = 5pF$		t_{PHZ}	-	25,0	ns
Low level to high impedance (output disable)	$C_L = 5pF$		t_{PLZ}	-	25,0	ns

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance