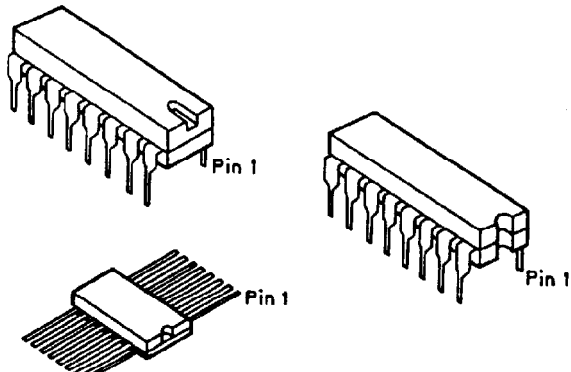


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 061 ISSUE 1 JULY 1981
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	 Page 1 of 18 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS148 64LS148 74LS148 84LS148 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	8-LINE TO 3-LINE OCTAL PRIORITY ENCODERS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS									OUTPUTS				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

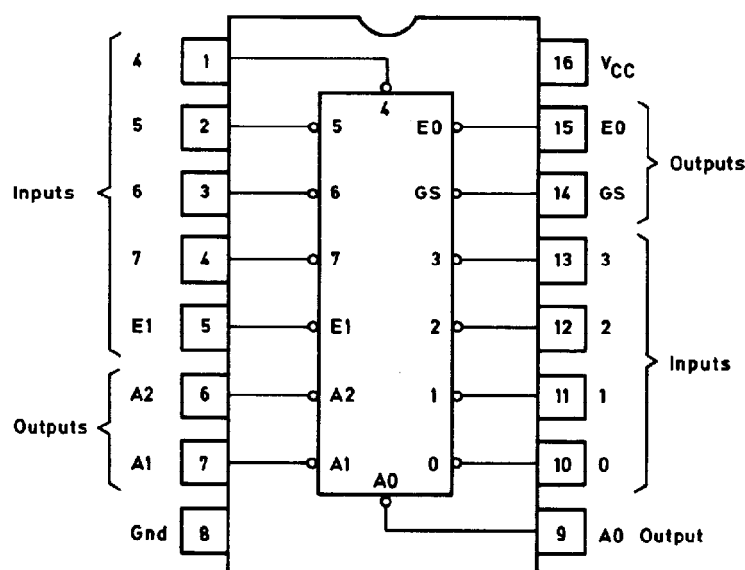
H = High level

L = Low level

X = Logic level irrelevant

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



8-line to 3-line octal priority encoders

The encoder features priority decoding of the inputs to ensure that only the highest order data line is encoded. The encoders encode eight data lines to three line Binary (octal). Cascading circuitry (enable input E1 and enable output EO) has been provided to allow octal expansion without the need for external circuit. Data inputs and outputs are active at the low level. All inputs are buffered to represent the one normalised TTL low power Schottky load. Output GS can be utilised to produce a priority flag when two LS148 devices are wired to provide 16-line to 4-line encoding.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS148J	N	W
-25 + 85	84LS148J		
-40 + 85	64LS148J		
-55 +125	54LS148J		

1.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.4 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1 Maximum continuous supply voltage V_{CC} -0,5V
+7,0V

2.2 Maximum input voltages

2.2.1 Maximum input voltage V_I -0,5V
+7,0V

2.2.2 Maximum input voltage between multiple emitter transistor inputs V_{II} +5,5V

			54LS	64LS	74LS	84LS
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55	-40	0	-25
			max. +125	+85	+70	+85

2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65	(All types)
			max. +150	

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,8	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	Condition 1**	V_{CC} max.	$I_{CC(1)}$	-	20,0	mA
	Condition 2**		$I_{CC(2)}$	-	17,0	mA
High level input current						
Inputs 1 through 7	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,2	mA
All other inputs				-	0,1	mA
Inputs 1 through 7	$V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(2)}$	-	40,0	μA
All other inputs				-	20,0	μA
Low level input current						
Inputs 1 through 7	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,8	mA
All other inputs				-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage 54LS	$I_{OH} = -400,0\mu A$	V_{CC} min.	V_{OH}	2,5	-	V
64/74/84LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
All types	$I_{OL(1)} = 4,0mA$ (1)		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA$ (2)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ (3) $V_{IL} = 0V$ or $4,5V$	V_{CC} max.	$-I_{OS}$	15,0	130,0	mA
Propagation times	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
All types						
High to Low level						
0 through 7 to AO, A1 or A2 (in phase)			t_{PHL}	-	25,0	ns
0 through 7 to AO, A1 or A2 (out of phase)			t_{PHL}	-	29,0	ns
0 through 7 to EO (out of phase)			t_{PHL}	-	40,0	ns
0 through 7 to GS (in phase)			t_{PHL}	-	21,0	ns
E1 to AO, A1 or A2 (in phase)			t_{PHL}	-	25,0	ns
E1 to GS (in phase)			t_{PHL}	-	36,0	ns
E1 to EO (in phase)			t_{PHL}	-	35,0	ns

(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1$ sec

*See 3.2.1 of this specification

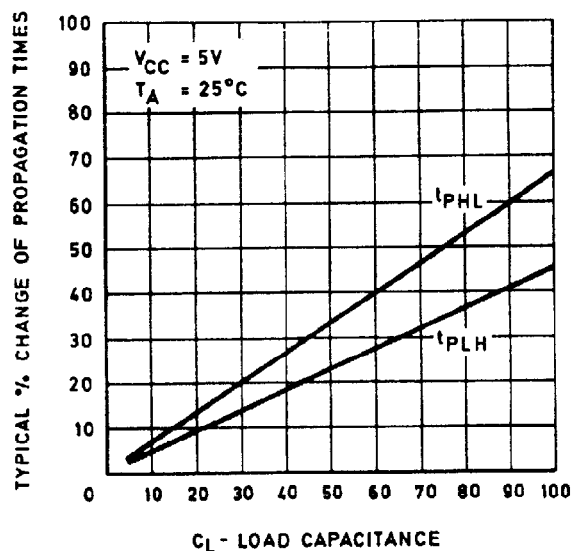
**See Sub-group A3 for conditions

3.2.2 (Contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Propagation times (contd)						
Low to High level						
0 through 7 to A0, A1 or A2 (in phase)			t_{PLH}	-	18,0	ns
0 through 7 to A0, A1 or A2 (out of phase)			t_{PLH}	-	36,0	ns
0 through 7 to E0 (out of phase)			t_{PLH}	-	18,0	ns
0 through 7 to GS (in phase)			t_{PLH}	-	55,0	ns
E1 to A0, A1 or A2 (in phase)			t_{PLH}	-	25,0	ns
E1 to GS (in phase)			t_{PLH}	-	17,0	ns
E1 to E0 (in phase)			t_{PLH}	-	21,0	ns

3. Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance