

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90103 - 070

ISSUE 1

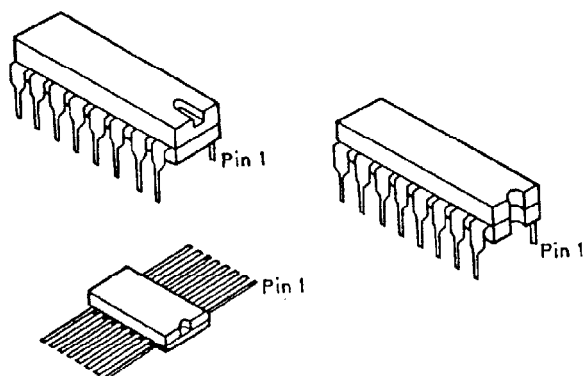
JANUARY 1982



Page 1 of 21 pages

ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54LS163A
64LS163A
74LS163A
84LS163AOutline not to scale: Isometric projection
Marking information see clause 1SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1Refer to IEC 191-1-50a (type A50C)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)BINARY SYNCHRONOUS CLEAR
4-BIT DIRECT COUNTERSTYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR TTL-LOW-POWER
SCHOTTKYASSESSMENT LEVELS
R, S, T AND V1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

- 1 -

CECC*90 103-070*IS*1 82 1974499 0008441 68T



Documents

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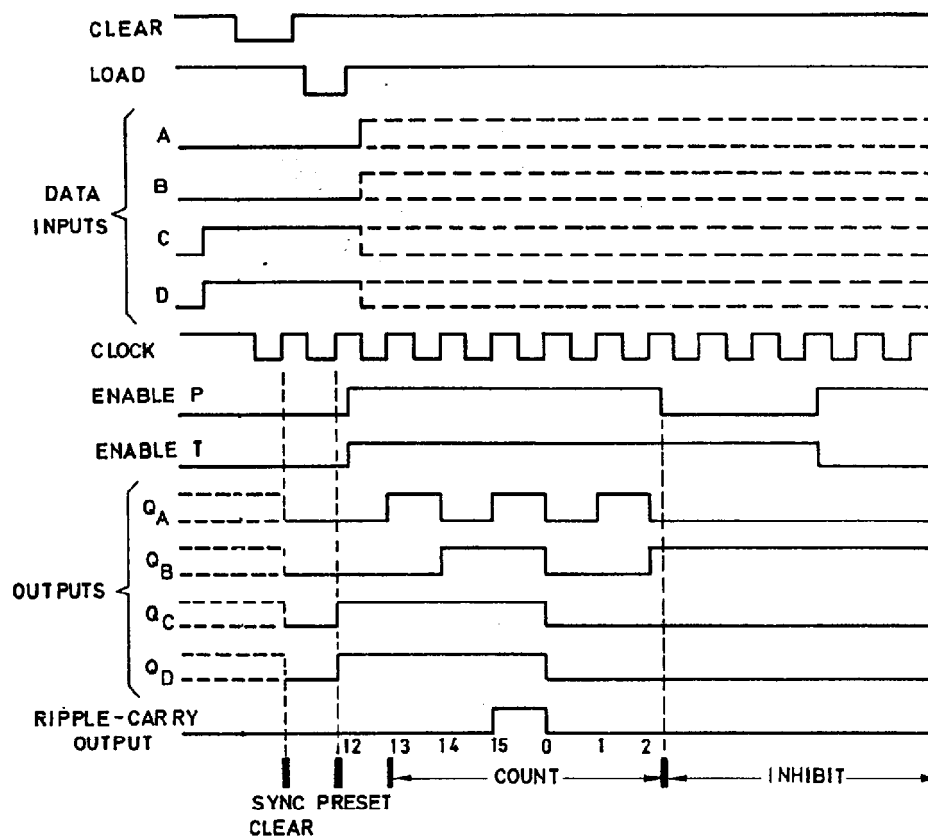
INPUTS										OUTPUTS			
CLEAR	LOAD	DATA				ENABLE		CLOCK	CARRY	Q _A	Q _B	Q _C	Q _D
		A	B	C	D	T	P						
L	H	L	L	L	L	L	L		L	L	L	L	L
H	H	L	L	L	L	H	H	H	L	L	L	L	L
H	H	L	L	L	L	H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H		L	H	L	L	L
H	H	L	L	L	L	H	H		L	L	L	L	L
These conditions are applied for a further 13 clock pulses										Outputs follow binary count sequence to count of 15			
H	H	L	L	L	L	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	L	H	L	H	H	H	H
H	L	L	L	L	L	L	L	L	L	H	H	H	H
H	L	L	L	L	L	L	L		L	L	L	L	L
H	L	H	L	L	L	L	L		L	H	L	L	L
H	L	Data inputs follow binary count sequence to count of 14				L	L		L	Outputs follow binary count sequence after each clock pulse			
H	L	H	H	H	H	H	L		H	H	H	H	H
H	H	H	H	H	H	L	H		L	H	H	H	H
H	H	L	L	L	L	H	L		H	H	H	H	H
H	H	L	L	L	L	H	H	H	H	H	H	H	H
H	H	L	L	L	L	H	H		L	L	L	L	L

 = High level clock pulse

H = High level

L = Low level

1.1.1 Typical operation timing diagram (typical Clear, Preset, Count and Inhibit sequences)



1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification

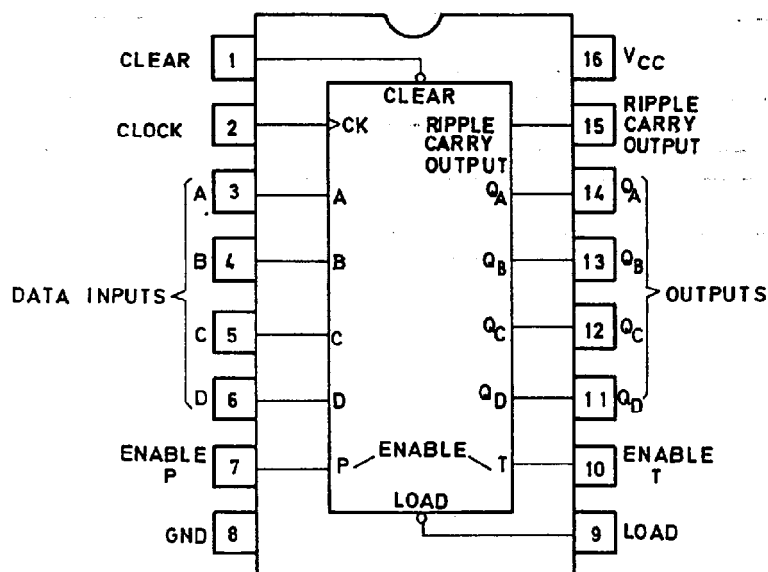
The counter is a 4-bit binary counter incorporating a 'Carry' circuit. Synchronous operation is provided by simultaneous clocking of the four J-K bistables, this arrangement causing the outputs to change coincident with each other when so ordered by the Count Enable inputs and internal gating. A buffered Clock input triggers the four bistables on its transition from Low to High.

Outputs may be preset by setting the Data inputs to the desired output levels, while the Load input is Low, and taking the Clock from Low to High. During presetting, the levels of the Enabling inputs are disregarded and the Low at the Load input disables the counter. Low to High transitions at the Load input should be avoided when the Clock input is Low if the Enable inputs are High at, or before, the Load input transition.

The 'Carry' circuit allows counters to be cascaded without additional gating. The signals associated with this circuit are the two Count Enable inputs (P and T) and a Ripple Carry output. When the counter reaches its maximum count with both Count Enable inputs High (both must be high for the counter to count) input T enables the Ripple Carry output which produces a High output pulse. This pulse can be used to enable succeeding cascaded stages.

A Low at the Clear input sets all four bistable outputs Low after the succeeding Clock pulse, regardless of the states of the Enable inputs.

1.2.1 Terminal identification (contd)



Binary synchronous clear 4-bit direct counters

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS163AJ	N	W
-25 + 85	84LS163AJ		
-40 + 85	64LS163AJ		
-55 +125	54LS163AJ		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}		-0,5V +7,0V
2.2	Maximum input voltages			
2.2.1	Maximum input voltage	V_I		-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}		+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	54LS -40 64LS +85 74LS 0 84LS -25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	I_{CCL} is measured with load input High, then with load input Low. All other inputs High, all outputs open.	V_{CC} max.	I_{CCL}	-	32,0	mA
	I_{CCH} is measured with clock input High, then with clock input Low. All other inputs Low, all outputs open.		I_{CCH}	-	31,0	mA
High level input current Data and enable P Load Clock and enable T Clear	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
			$I_{IH(1)}$	-	0,2	mA
			$I_{IH(1)}$	-	0,2	mA
Data and enable P Load Clock and enable T Clear	$V_{IH(2)}$		$I_{IH(2)}$	-	20,0	µA
			$I_{IH(2)}$	-	40,0	µA
			$I_{IH(2)}$	-	40,0	µA
Low level input current Data and enable P Load Clock and enable T Clear	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
			$-I_{IL}$	-	0,8	mA
			$-I_{IL}$	-	0,8	mA

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage						
54LS	$I_{OH} = -400,0\mu A$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
64/74/84LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
All types	$I_{OL(1)} = 4,0mA \quad (1)$		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA \quad (2)$		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V \quad (3)$ $V_{IN} = 0 \text{ or } 4,5V\ddagger$	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation time	$T_{amb} = 25^\circ C^*$	5,0V				
All types	test conditions as in Sub-group A5					
High to Low level						
Clock to Ripple Carry output			t_{PHL}	-	35,0	ns
Clock to each Q output	(Load input High)		t_{PHL}	-	27,0	ns
Clock to each Q output	(Load input Low)		t_{PHL}	-	27,0	ns
Enable T to Ripple Carry output			t_{PHL}	-	15,0	ns
Clear to each Q output**			t_{PHL}	-	35,0	ns
Low to High level						
Clock to Ripple Carry output			t_{PLH}	-	35,0	ns
Clock to each Q output	(Load input High)		t_{PLH}	-	24,0	ns
Clock to each Q output	(Load input Low)		t_{PLH}	-	18,0	ns
Data hold time			t_{hold}	0	-	ns
Maximum clock frequency			f_{clock}	25,0	-	MHz
Duration of clock pulse			$t_{p(clock)}$	25,0	-	ns
Duration of clear pulse			$t_{p(clear)}$	20,0	-	ns
Set-up time			t_{set-up}	20,0	-	ns
Data Load, Enable and Clear inputs						

(1) Fan out = 10, (2) Fan out = 20

(3) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See Clause 3 of this specification

**Measured from the positive clock transition

 $\ddagger$ Refer to truth table