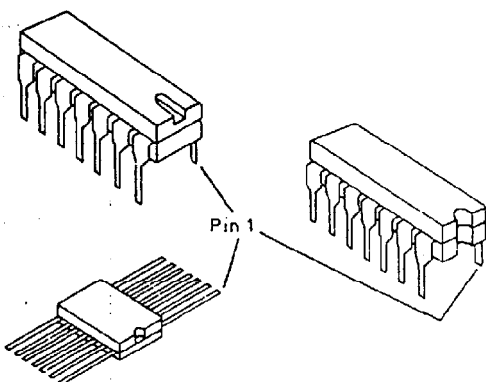


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 071 ISSUE 1 JANUARY 1982  Page 1 of 19 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS164 64LS164 74LS164 84LS164 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50B) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTERS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description
 - 1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	$Q_B \dots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	↑	H	H	H	Q_{AN}	Q_{GN}
H	↑	L	X	L	Q_{AN}	Q_{GN}
H	↑	X	L	L	Q_{AN}	Q_{GN}

H = High level

L = Low level

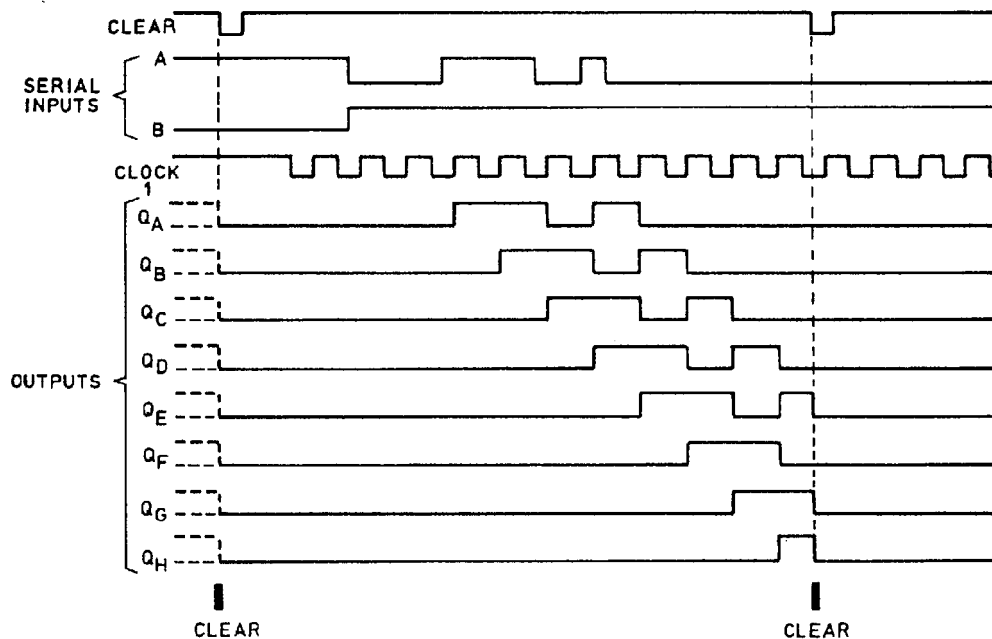
↑ = Positive clock transition

X = Logic level irrelevant

 Q_{AO} , Q_{BO} etc. = The output logic level before the indicated steady level conditions were applied $Q_{AN} \dots Q_{GN}$ = The output logic level before the most recent positive clock transition.

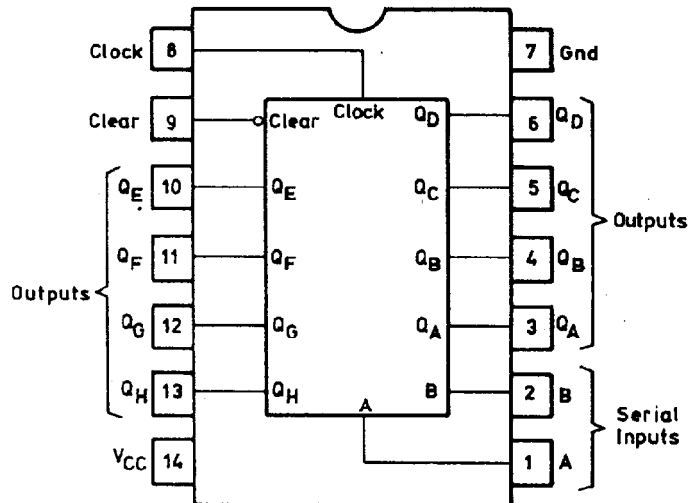
Serial data is entered on the positive transition of the clock pulse. A Low level at either or both Serial inputs inhibits the entry of data and sets the Q_A output Low on the next positive Clock transition. A High level on one of the Serial inputs enables the other Serial output.

1.1.1 Typical operation timing diagram
(typical clear, shift and clear sequences)



1.2 Terminal identification, type designation and marking.

1.2.1 Terminal identification



The register is an 8-bit parallel-out serial shift register incorporating gated Serial inputs (A and B) and an asynchronous Clear. The gated serial inputs permit complete control over incoming data as a Low at either input, or at both inputs, inhibits entry of new data and resets the first of the eight bistables to Low at the succeeding Clock pulse. Either of the Serial inputs at High enables the other input which then determine the level of the first bistable.

Change of data at the Serial inputs may be affected only when the Clock is High or Low. Clocking of the bistables occurs on the Low to High transition of the Clock input. All inputs are diode clamped to minimise transmission-line effects.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS164J	N	W
-25 + 85	84LS164J		
-40 + 85	64LS164J		
-55 +125	54LS164J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}		-0,5V	+7,0V		
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I		-0,5V	+7,0V		
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}		+5,5V			
						54LS	64LS 74LS 84LS
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	-55	-40	0	-25
			max.	+125	+85	+70	+85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)		
			max.	+150			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

3.1 (contd)

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IL} = 0V$ (1) $V_{IH} = 4,5V$	$V_{CC} \text{ max.}$	I_{CC}	-	27,0	mA
High level input current	$V_{IH(1)} = 7,0V$ $V_{IH(2)} = 2,7V$	$V_{CC} \text{ max.}$ $V_{CC} \text{ max.}$	$I_{IH(1)}$ $I_{IH(2)}$	- -	100,0 20,0	μA μA
Low level input current	$V_{IL} = 0,4V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage	$I_{OH} = -400,0\mu A$ $I_{OH} = -400,0\mu A$ All types 64/74/84LS $I_{OL(1)} = 4,0mA$ (2) $I_{OL(2)} = 8,0mA$ (3)	$V_{CC} \text{ min.}$	V_{OH} V_{OH} $V_{OL(1)}$ $V_{OL(2)}$	2,5 2,7 - -	- - 0,4 0,5	V V V V
Output short circuit current	$V_O = 0V$ (4) $V_{IL} = 0V$	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times All types	$T_{amb} = 25^{\circ}C$ test conditions as in Sub-group A5	5,0V				
High to Low level						
Clear inputs to outputs			t_{PHLA}	-	36,0	ns
Clock inputs to outputs			t_{PHLA}	-	32,0	ns
Low to High level Clock inputs to outputs			t_{PLHA}	-	27,0	ns
Frequency of operation			$f_{max.}$	-	25,0	MHz
Duration of Clock pulse			$t_{p(clock)}$	20,0	-	ns
Duration of Clear pulse			$t_{p(clear)}$	20,0	-	ns
Data set-up time (see Appendix A1.3)			$t_{pset-up}$	15,0	-	ns
Data hold time			t_{hold}	5,0	-	ns

(1) To all inputs, (2) Fan out = 10, (3) Fan out = 20,

(4) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See 3.2.1 of this specification