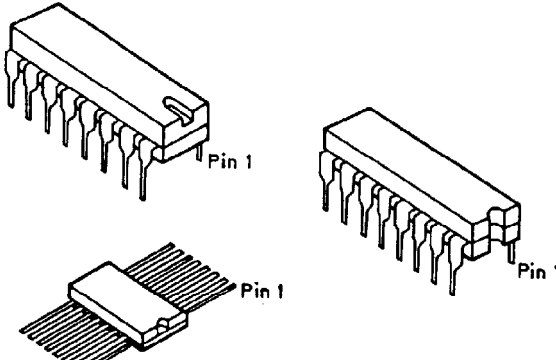


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 072 ISSUE 1 NOVEMBER 1981 Page 1 of 19 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	 MANUFACTURERS TYPE NUMBER 54LS165 64LS165 74LS165 84LS165 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	PARALLEL-LOAD 8-BIT SHIFT REGISTERS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q _A	Q _B	Q _H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q _{AO}	Q _{BO}	Q _{HO}
H	L	↑	H	X	H	Q _{AO}	Q _{GO}
H	L	↑	L	X	L	Q _{AO}	Q _{GO}
H	H	X	X	X	Q _{AO}	Q _{BO}	Q _{HO}

Q_{AN} = Data previously at Q_A now shifted one bit to Q_B output

Q_{AO} = Level of Q_A before the indicated steady level input conditions were established

↑ = Transition from Low to High level

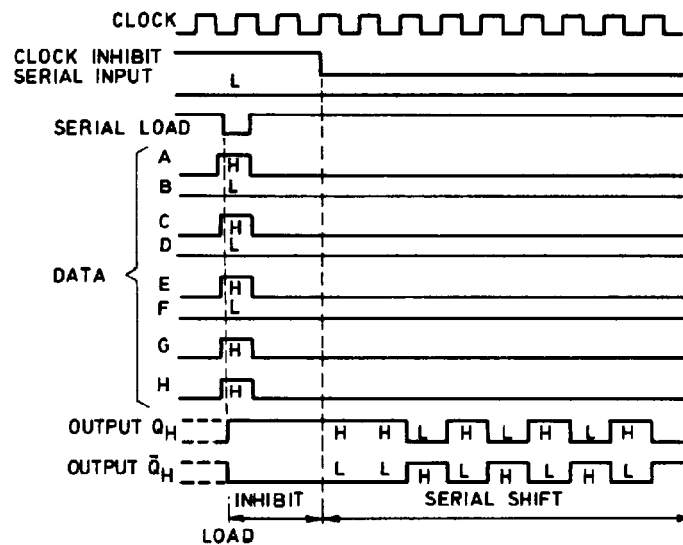
a = Data entered on input A or output Q_A

H = High level

L = Low level

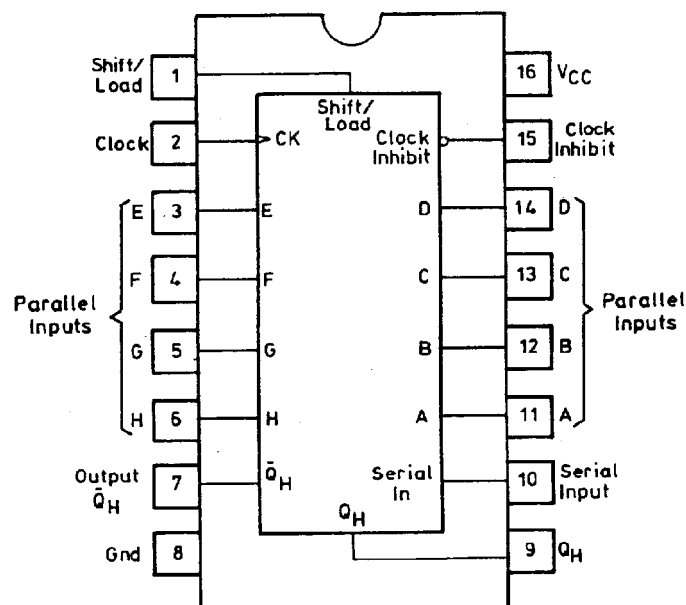
X = Logic level irrelevant

1.1.1 Typical operation timing diagram (typical shift, load and inhibit sequences)



1.2 Terminal identification, type designation and marking.

1.2.1 Terminal identification



Parallel - load 8-bit shift register

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS165J	N	W
-25 + 85	84LS165J		
-40 + 85	64LS165J		
-55 +125	54LS165J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
				54LS	64LS	74LS	84LS	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

3.1 (contd)

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
D.C. noise margin				
Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
High level ($V_{IHB} - V_{OHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	Outputs open Clock inhibit and clock 4,5V Clock pulse applied to shift/load input I_{CC} measured first with parallel inputs 4,5V then parallel inputs 0V	V_{CC} max.	I_{CC}	-	36,0	mA
High level input current	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,3	mA
Shift/Load			$I_{IH(1)}$	-	0,1	mA
Other inputs	$V_{IH(2)} = 2,7V$		$I_{IH(2)}$	-	60,0	μA
Shift/Load			$I_{IH(2)}$	-	20,0	μA
Other inputs						
Low level input current	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	1,2	mA
Shift/Load			$-I_{IL}$	-	0,4	mA
Other inputs						
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage	$I_{OH} = -400,0\mu A$	V_{CC} min.	V_{OH}	2,5	-	V
54LS			V_{OH}	2,7	-	V
64/74/84LS						
All types	$I_{OL(1)} = 4,0mA$ (1)		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA$ (2)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ (3) $V_{IL} = 0V$ or 4,5V	V_{CC} max.	$-I_{OS}$	15,0	130,0	mA
Propagation times	$T_{amb} = 25^{\circ}C$ test conditions as in Sub-group A5	5,0V				
All types						
High to Low level			t_{PHLA}	-	40,0	ns
From Clock to Any			t_{PHLA}	-	35,0	ns
Load to Any			t_{PHLA}	-	30,0	ns
H to Q_H			t_{PHLA}	-	25,0	ns
H to $\overline{Q}_H$						

(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1$ sec

*See 3.2.1 of this specification