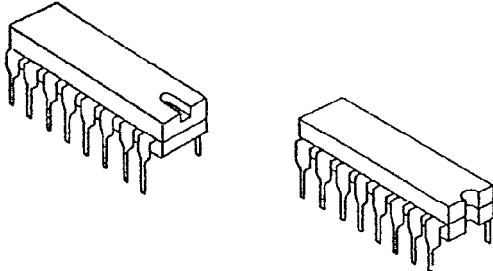


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103-073 ISSUE 1 OCTOBER 1982  Page 1 of 1 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND <i>family specification for TTL</i> <i>Low-power-schottky-circuits</i> (BS CECC 90103)	MANUFACTURERS TYPE NUMBER 54LS166A 64LS166A 74LS166A 84LS166A SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977 Outline not to scale: Isometric projection Marking information see clause 1  For detail dimensions BS 3934 SO-87C	<i>Detail specification for parallel load 8-bit shift register.</i> TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL Low-power Schottky ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200 for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q _A	Q _B	Q _H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q _{AO}	Q _{BO}	Q _{HO}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q _{AN}	Q _{HN}
H	H	L	↑	L	X	L	Q _{AN}	Q _{HN}
H	X	H	↑	X	X	Q _{AO}	Q _{BO}	Q _{HO}

Q_{AN} = Data previously at Q_A now shifted one bit to Q_B output

Q_{AO} = Level of Q_A before the indicated steady level input conditions were established

↑ = Transition from Low to High level

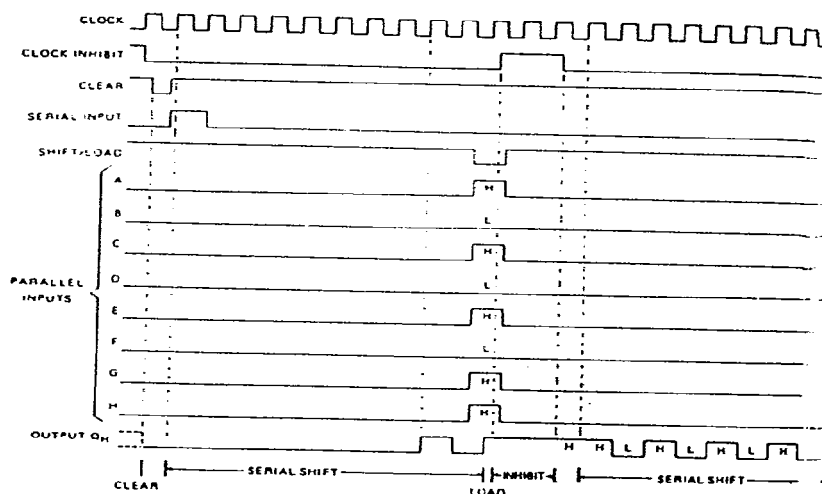
a = Data entered on input A or output Q_A

H = High level

L = Low level

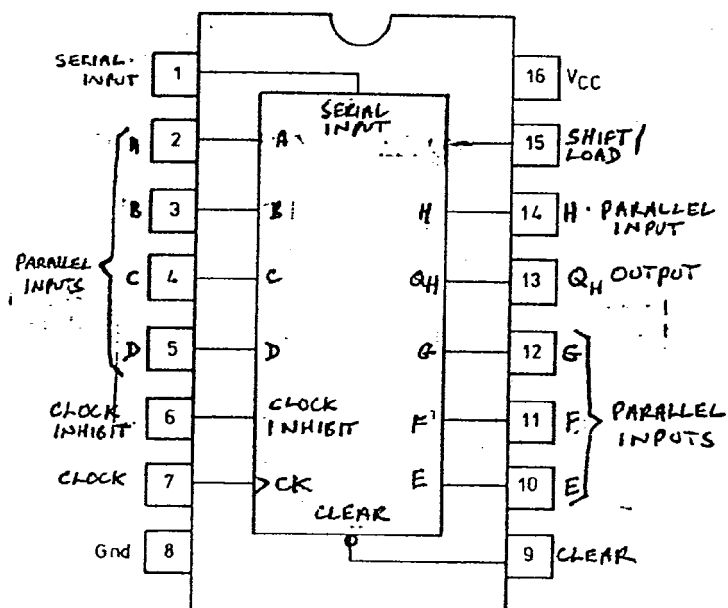
X = Logic level irrelevant

1.1.1 Typical operation timing diagram (typical shift, load and inhibit sequences)



1.2 Terminal identification, type designation and marking.

1.2.1 Terminal identification



Parallel - load 8-bit shift register

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS166AJ	N	W
-25 + 85	84LS166AJ		
-40 + 85	64LS166AJ		
-55 +125	54LS166AJ		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}		-0,5V	+7,0V		
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I		-0,5V	+7,0V		
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}		+5,5V			
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	-55	-40	0	-25
			max.	+125	+85	+70	+85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)		
			max.	+150			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

3.1 (contd)

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
D.C. noise margin				
Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
High level ($V_{IHB} - V_{OHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+35	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	Outputs open Serial input 4,5V all other inputs except the clock grounded. <i>I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.</i>	$V_{CC} \text{ max.}$	I_{CC}	-	32,0	mA
High level input current	$V_{IH(1)} = 7,0V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,1	mA
	$V_{IH(2)} = 2,7V$		$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage 54LS 64/74/84LS All types 64/74/84LS	$I_{OH} = -400,0\mu A$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
	$I_{OL(1)} = 4,0mA \quad (1)$		$V_{OL(1)}$	-	0,4	V
	$I_{OL(2)} = 8,0mA \quad (2)$		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V \quad (3)$ $V_{IL} = 0V \text{ or } 4,5V$	$V_{CC} \text{ max.}$	$-I_{OS}$	20,0	100,0	mA
Propagation times All types	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
High to Low level From Clock to Any clear to Any			t_{PHLA}	7	25,0	ns
			t_{PHLA}	-	30,0	ns

(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See 3.2.1 of this specification