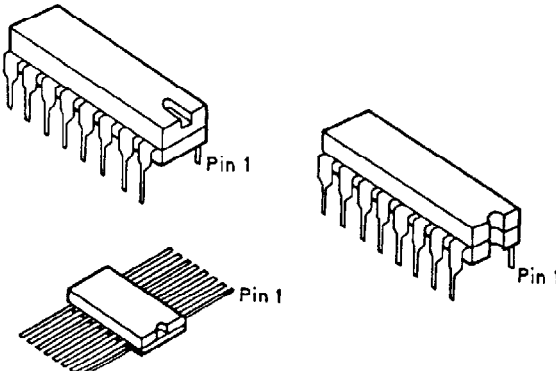


|                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                          |                                                                                                                                             |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| <b>BRITISH STANDARDS INSTITUTION</b><br>2 PARK STREET, LONDON. W1A 2BS                                                                                                                                                                                                                                           | BS CECC 90103 - 075<br><br>ISSUE 1<br><br>JULY 1981<br><br><br><br>Page 1 of 21 pages | ELECTRONIC COMPONENTS OF ASSESSED QUALITY<br>DETAIL SPECIFICATION IN ACCORDANCE WITH:<br><br>BS CECC 90 000 : 1976<br>BS CECC 90 100 : 1977 |
| Outline not to scale: Isometric projection<br>Marking information see clause 1<br><br><br><br>Refer to IEC 191-1-50a (type A50C)<br>Dual-in-Line (plastic or ceramic)<br>refer to Appendix A1.3<br>Flatpack (metal or ceramic) | <b>MANUFACTURERS TYPE NUMBER</b><br><br>54LS170<br>64LS170<br>74LS170<br>84LS170<br><br>SEE PD 9002 AND CECC 00 200<br>For ordering information see clause 1             | 4 x 4 REGISTER FILE WITH<br>OPEN COLLECTOR OUTPUTS                                                                                          |
|                                                                                                                                                                                                                                                                                                                  | TYPICAL CONSTRUCTION<br>SILICON MONOLITHIC<br>BIPOLAR TTL-LOW-POWER<br>SCHOTTKY                                                                                          | <b>ASSESSMENT LEVELS</b><br>R, S, T AND V                                                                                                   |

# 1. Type description

## 1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200 for details of manufacturers approved to this specification

## 1.1 Truth table (contd)

Data input test pattern

| 1D | 2D | 3D | 4D |
|----|----|----|----|
| L  | L  | L  | L  |
| L  | L  | L  | H  |
| L  | L  | H  | L  |
| L  | L  | H  | H  |
| L  | H  | L  | L  |
| L  | H  | L  | H  |
| L  | H  | H  | L  |
| L  | H  | H  | H  |
| H  | L  | L  | L  |
| H  | L  | L  | H  |
| H  | L  | H  | L  |
| H  | L  | H  | H  |
| H  | H  | L  | L  |
| H  | H  | L  | H  |
| H  | H  | H  | L  |
| H  | H  | H  | H  |

For Write truth table see notes a,b,c and d

| WRITE INPUTS   |                |                | WORD           |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| W <sub>B</sub> | W <sub>A</sub> | G <sub>W</sub> | 0              | 1              | 2              | 3              |
| L              | L              | L              | Q=D            | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |
| L              | H              | L              | Q <sub>0</sub> | Q=D            | Q <sub>0</sub> | Q <sub>0</sub> |
| H              | L              | L              | Q <sub>0</sub> | Q <sub>0</sub> | Q=D            | Q <sub>0</sub> |
| H              | H              | L              | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> | Q=D            |
| X              | X              | H              | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |

For Read truth table see notes a and d

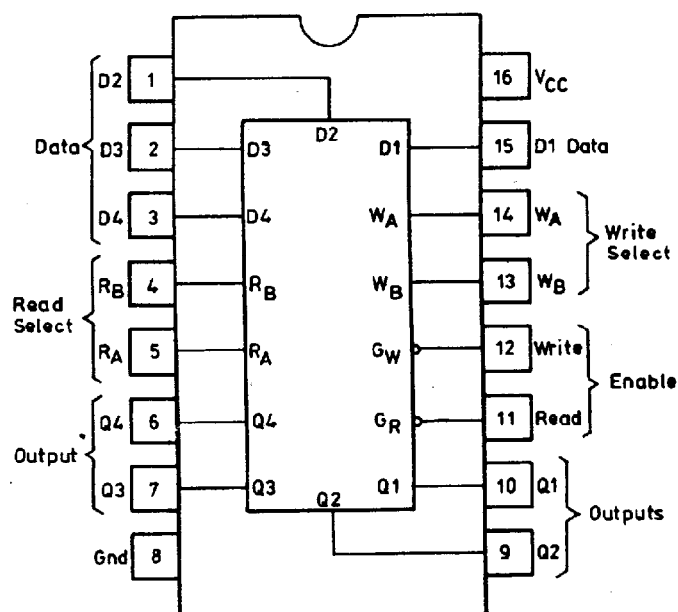
| READ INPUTS    |                |                | OUTPUTS        |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| R <sub>B</sub> | R <sub>A</sub> | G <sub>R</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> | Q <sub>4</sub> |
| L              | L              | L              | WOB1           | WOB2           | WOB3           | WOB4           |
| L              | H              | L              | W1B1           | W1B2           | W1B3           | W1B4           |
| H              | L              | L              | W2B1           | W2B2           | W2B3           | W2B4           |
| H              | H              | L              | W3B1           | W3B2           | W3B3           | W3B4           |
| X              | X              | H              | H              | H              | H              | H              |

## NOTES:

- H = High level  
L = Low level  
X = Logic level irrelevant
- (Q=D) = The four selected internal bistable outputs will assume the levels applied to the four external data inputs
- Q<sub>0</sub> = The level of Q before the indicated input conditions were established
- WOB1 = The first bit of word 0. etc.
- D = 1D, 2D, 3D and 4D (see Data input test pattern)
- G<sub>R</sub>, G<sub>W</sub> = Read/write enable inputs respectively

## 1.2 Terminal identification, type designation and marking

## 1.2 Terminal identification



## 4 x 4 register file with open collector outputs

The register file is organised as four 4-bit words. Decoding is provided for addressing the four word locations to either write-in or read-out data, thus permitting simultaneous writing into one location and reading from another.

The four data inputs (D1-D4) supply the word to be stored, the store location being determined by the Write Select inputs ( $W_A$ ,  $W_B$ ). Data applied at the Data inputs should be in its true form, i.e. if a High level signal is required at an output ( $Q1-Q4$ ), the data input for the associated bit location must also be High. New data is accepted only if both internal address gate inputs are High. When this condition exists, data at the D input is transferred to the output. When the Write Enable input (GW) is High, the Data inputs are inhibited and, therefore, can cause no change in the stored information. When the Read Enable input (GR) is High, the Data outputs are inhibited and remain High.

Individual address (Select) lines allow direct acquisition of data in any of the four store locations, four decoding gates being used to complete the address for reading a word. When the read address is presented at the Read Select inputs ( $R_A$ ,  $R_B$ ) and the Read Enable signal is present at  $G_R$ , the 4-bit word is read from its location and appears at the outputs.

The register file has a non-destructive readout in that data is not lost when addressed.

## 1.2.2 Type designation

| TEMPERATURE<br>RANGE | PACKAGE                 |                         |                     |
|----------------------|-------------------------|-------------------------|---------------------|
|                      | Ceramic<br>Dual-in-Line | Plastic<br>Dual-in-Line | Ceramic<br>Flatpack |
| 0 + 70               | 74LS170J                | N                       | W                   |
| -25 + 85             | 84LS170J                |                         |                     |
| -40 + 85             | 64LS170J                |                         |                     |
| -55 +125             | 54LS170J                |                         |                     |

## 1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

## 1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

|     |                                                    |                      |                       |             |          |            |                |
|-----|----------------------------------------------------|----------------------|-----------------------|-------------|----------|------------|----------------|
| 2.1 | Maximum continuous supply voltage                  | $V_{CC}$             |                       |             |          |            | -0,5V<br>+7,0V |
| 2.2 | Maximum input voltage                              | $V_I$                |                       |             |          |            | -0,5V<br>+7,0V |
|     |                                                    |                      | 54LS                  | 64LS        | 74LS     | 84LS       |                |
| 2.3 | Minimum and maximum operating ambient temperatures | $T_{amb}(^{\circ}C)$ | min. -55<br>max. +125 | -40<br>+85  | 0<br>+70 | -25<br>+85 |                |
| 2.4 | Minimum and maximum storage temperatures           | $T_{stg}(^{\circ}C)$ | min. -65<br>max. +150 | (All types) |          |            |                |

### 3. Recommended operating conditions and associated characteristics (not for inspection purposes)

#### 3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

| Description                                                           | Symbol     | Type               | Value                    | Unit     |
|-----------------------------------------------------------------------|------------|--------------------|--------------------------|----------|
| Positive supply voltage range                                         | $V_{CC}$   | 54LS<br>64/74/84LS | 4,5 - 5,5<br>4,75 - 5,25 | V<br>V   |
| Minimum value of High level input voltage                             | $V_{IHB}$  | All types          | 2,0                      | V        |
| Maximum value of High level input voltage                             | $V_{IHA}$  | All types          | 5,5                      | V        |
| Minimum value of Low level input voltage                              | $V_{ILB}$  | All types          | -0,3                     | V        |
| Maximum value of Low level input voltage                              | $V_{ILA}$  | 54LS<br>64/74/84LS | 0,7<br>0,8               | V<br>V   |
| Maximum value of Low level output current for each output             | $I_{OLA}$  | 54LS<br>64/74/84LS | 4,0<br>8,0               | mA<br>mA |
| Maximum value of output current (leakage) for each output at $V_{OH}$ | $I_{OHXA}$ | All types          | 100,0                    | $\mu A$  |
| Maximum value of applied off-state output voltage                     | $V_{OHA}$  | All types          | 5,5                      | V        |

#### 3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (\*)

|                       | 54LS | 64LS | 74LS | 84LS |    |
|-----------------------|------|------|------|------|----|
| T <sub>amb</sub> min. | -55  | -40  | 0    | -25  | °C |
| T <sub>amb</sub> max. | +125 | +85  | +70  | +85  |    |
| V <sub>CC</sub> min.  | 4,5  | 4,75 |      |      | V  |
| V <sub>CC</sub> max.  | 5,5  | 5,25 |      |      |    |

## 3.2.2

| Characteristics                               | Conditions                                                                                                              | V <sub>CC</sub> (V)  | Symbol                  | Min.                                                                                                                 | Max.                 | Unit             |   |     |    |
|-----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|----------------------|-------------------------|----------------------------------------------------------------------------------------------------------------------|----------------------|------------------|---|-----|----|
| Total supply current per package              | V <sub>IN</sub> = 4,5V to all Data and Enable inputs.<br><br>Address inputs = 0V<br>Outputs open circuit                | V <sub>CC</sub> max. | I <sub>CC</sub>         | -                                                                                                                    | 40,0                 | mA               |   |     |    |
| High level input current                      | V <sub>IN(1)</sub> = 7,0V to input under test<br>other inputs open circuit<br><br>Any D,R or W input<br>GR or GW inputs | V <sub>CC</sub> max. | I <sub>IH(1)</sub>      | -                                                                                                                    | 100,0                | µA               |   |     |    |
|                                               |                                                                                                                         |                      | I <sub>IH(1)</sub>      | -                                                                                                                    | 200,0                | µA               |   |     |    |
|                                               | V <sub>IN(2)</sub> = 2,7V to input under test<br>other inputs open circuit<br><br>Any D,R or W input<br>GR or GW inputs |                      | I <sub>IH(2)</sub>      | -                                                                                                                    | 20,0                 | µA               |   |     |    |
|                                               |                                                                                                                         |                      | I <sub>IH(2)</sub>      | -                                                                                                                    | 40,0                 | µA               |   |     |    |
|                                               |                                                                                                                         |                      | Low level input current | V <sub>IN</sub> = 0,4V to input under test<br>other inputs open circuit<br><br>Any D,R or W input<br>GR or GW inputs | V <sub>CC</sub> max. | -I <sub>IL</sub> | - | 0,4 | mA |
|                                               |                                                                                                                         |                      |                         |                                                                                                                      |                      | -I <sub>IL</sub> | - | 0,8 | mA |
| Output voltage<br><br>All types<br>64/74/84LS | I <sub>OL(1)</sub> = 4,0mA (1)<br>I <sub>OL(2)</sub> = 8,0mA (2)                                                        | V <sub>CC</sub> min. | V <sub>OL(1)</sub>      | -                                                                                                                    | 0,4                  | mA               |   |     |    |
|                                               |                                                                                                                         |                      | V <sub>OL(2)</sub>      | -                                                                                                                    | 0,5                  | mA               |   |     |    |
| Propagation times<br><br>All types            | T <sub>amb</sub> = 25°C*<br>test conditions as in Sub-group A5                                                          | 5,0V                 | t <sub>PHL</sub>        | -                                                                                                                    | 30,0                 | ns               |   |     |    |
| Read Enable to any output                     | -                                                                                                                       |                      |                         | 40,0                                                                                                                 | ns                   |                  |   |     |    |
| Read Select to any output                     | -                                                                                                                       |                      |                         | 40,0                                                                                                                 | ns                   |                  |   |     |    |
| Write Enable to any output                    | -                                                                                                                       |                      |                         | 35,0                                                                                                                 | ns                   |                  |   |     |    |
| Data to any output                            | t <sub>PLH</sub>                                                                                                        |                      | -                       | 30,0                                                                                                                 | ns                   |                  |   |     |    |
| Read Enable to any output                     |                                                                                                                         |                      | -                       | 40,0                                                                                                                 | ns                   |                  |   |     |    |

(1) Fan out = 10, (2) Fan out = 20,

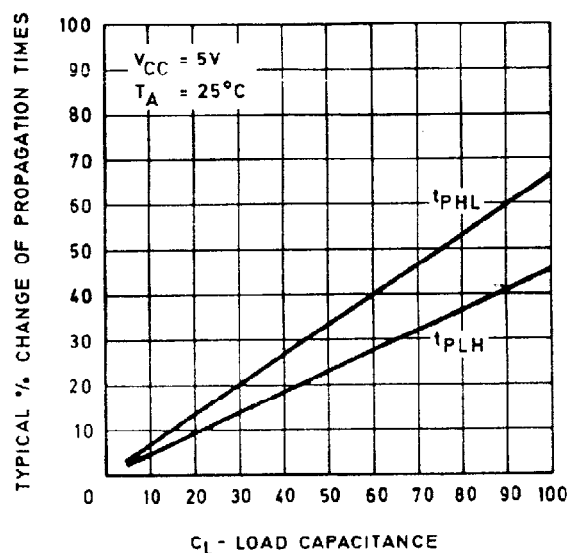
\*See 3.2.1 of this specification

## 3.2.2 (contd)

| Characteristics                      | Conditions | $V_{CC}(V)$ | Symbol            | Min. | Max. | Unit |
|--------------------------------------|------------|-------------|-------------------|------|------|------|
| Write Enable to any output           |            |             | $t_{PLH}$         | -    | 45,0 | ns   |
| Data to any output                   |            |             |                   | -    | 45,0 | ns   |
| Data set-up time w.r.t. Write Enable |            |             | $t_{(set-up)(D)}$ | 10,0 | -    | ns   |
| Write set-up time w.r.t Write Enable |            |             | $t_{(set-up)(W)}$ | 15,0 | -    | ns   |
| Data hold time w.r.t Write Enable    |            |             | $t_{(hold)(D)}$   | 15,0 | -    | ns   |
| Write hold time w.r.t Write Enable   |            |             | $t_{(hold)(W)}$   | 5,0  | -    | ns   |
| Write Recovery time                  |            |             | $t_{WR}$          | 25,0 | -    | ns   |
| Write or Read pulse duration         |            |             | $t_{P(W)}$        | 25,0 | -    | ns   |

## 3.3 Supplementary information

## 3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance