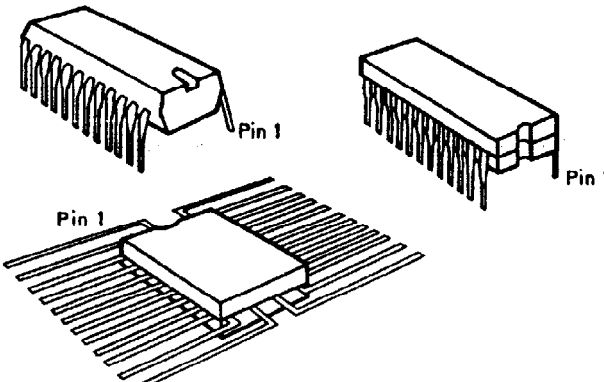


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	BS CECC 90103 - 078 ISSUE 1 NOVEMBER 1981 Page 1 of 24 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS181 64LS181 74LS181 84LS181
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A51D) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

TABLE A

SELECTION				ACTIVE LOW DATA		
				M = H LOGIC FUNCTIONS	M = L ARITHMETIC OPERATIONS	
					$C_n = L$ (no carry)	$C_n = H$ (with carry)
S3	S2	S1	S0			
L	L	L	L	$F = \bar{A}$	$F = A \text{ MINUS } 1$	$F = A$
L	L	L	H	$F = \bar{A}\bar{B}$	$F = AB \text{ MINUS } 1$	$F = AB$
L	L	H	L	$F = \bar{A} + B$	$F = \bar{A}\bar{B} \text{ MINUS } 1$	$F = \bar{A}\bar{B}$
L	L	H	H	$F = 1$	$F = \text{MINUS } 1 \text{ (2's COMP)}$	$F = \text{ZERO}$
L	H	L	L	$F = \overline{A + B}$	$F = A \text{ PLUS } (A + \bar{B})$	$F = A \text{ PLUS } (A + \bar{B}) \text{ PLUS } 1$
L	H	L	H	$F = \bar{B}$	$F = AB \text{ PLUS } (A + \bar{B})$	$F = AB \text{ PLUS } (A + \bar{B}) \text{ PLUS } 1$
L	H	H	L	$F = A \oplus B$	$F = A \text{ MINUS } B \text{ MINUS } 1$	$F = A \text{ MINUS } B$
L	H	H	H	$F = A + \bar{B}$	$F = A + \bar{B}$	$F = (A + \bar{B}) \text{ PLUS } 1$
H	L	L	L	$F = \bar{A}B$	$F = A \text{ PLUS } (A + B)$	$F = A \text{ PLUS } (A + B) \text{ PLUS } 1$
H	L	L	H	$F = A \oplus B$	$F = A \text{ PLUS } B$	$F = A \text{ PLUS } B \text{ PLUS } 1$
H	L	H	L	$F = B$	$F = \bar{A}\bar{B} \text{ PLUS } (A + B)$	$F = \bar{A}\bar{B} \text{ PLUS } (A + B) \text{ PLUS } 1$
H	L	H	H	$F = A + B$	$F = (A + B)$	$F = (A + B) \text{ PLUS } 1$
H	H	L	L	$F = 0$	$F = A \text{ PLUS } A^*$	$F = A \text{ PLUS } A \text{ PLUS } 1$
H	H	L	H	$F = \bar{A}\bar{B}$	$F = AB \text{ PLUS } A$	$F = AB \text{ PLUS } A \text{ PLUS } 1$
H	H	H	L	$F = AB$	$F = \bar{A}\bar{B} \text{ PLUS } A$	$F = \bar{A}\bar{B} \text{ PLUS } A \text{ PLUS } 1$
H	H	H	H	$F = A$	$F = A$	$F = A \text{ PLUS } 1$

* Each bit is shifted to the next more significant position

1.1 Truth table (contd)

TABLE B

SELECTION				ACTIVE HIGH DATA		
				M = H LOGIC FUNCTIONS	M = L ARITHMETIC OPERATIONS	
					$\overline{C}_n = H$ (no carry)	$\overline{C}_n = L$ (with carry)
S3	S2	S1	S0			
L	L	L	L	$F = \overline{A}$	$F = A$	$F = A \text{ PLUS } 1$
L	L	L	H	$F = \overline{A + B}$	$F = A + B$	$F = (A + B) \text{ PLUS } 1$
L	L	H	L	$F = \overline{AB}$	$F = A + \overline{B}$	$F = (A + \overline{B}) \text{ PLUS } 1$
L	L	H	H	$F = 0$	$F = \text{MINUS } 1 \text{ (2's COMPL)}$	$F = \text{ZERO}$
L	H	L	L	$F = \overline{AB}$	$F = A \text{ PLUS } \overline{AB}$	$F = A \text{ PLUS } \overline{AB} \text{ PLUS } 1$
L	H	L	H	$F = \overline{B}$	$F = (A + B) \text{ PLUS } \overline{AB}$	$F = (A + B) \text{ PLUS } \overline{AB} \text{ PLUS } 1$
L	H	H	L	$F = A \oplus B$	$F = A \text{ MINUS } B \text{ MINUS } 1$	$F = A \text{ MINUS } B$
L	H	H	H	$F = \overline{AB}$	$F = \overline{AB} \text{ MINUS } 1$	$F = \overline{AB}$
H	L	L	L	$F = \overline{A} + B$	$F = A \text{ PLUS } AB$	$F = A \text{ PLUS } AB \text{ PLUS } 1$
H	L	L	H	$F = \overline{A \oplus B}$	$F = A \text{ PLUS } B$	$F = A \text{ PLUS } B \text{ PLUS } 1$
H	L	H	L	$F = B$	$F = (A + \overline{B}) \text{ PLUS } AB$	$F = (A + \overline{B}) \text{ PLUS } AB \text{ PLUS } 1$
H	L	H	H	$F = AB$	$F = AB \text{ MINUS } 1$	$F = AB$
H	H	L	L	$F = 1$	$F = A \text{ PLUS } A^*$	$F = A \text{ PLUS } A \text{ PLUS } 1$
H	H	L	H	$F = A + \overline{B}$	$F = (A + B) \text{ PLUS } A$	$F = (A + B) \text{ PLUS } A \text{ PLUS } 1$
H	H	H	L	$F = A + B$	$F = (A + \overline{B}) \text{ PLUS } A$	$F = (A + \overline{B}) \text{ PLUS } A \text{ PLUS } 1$
H	H	H	H	$F = A$	$F = A \text{ MINUS } 1$	$F = A$

* Each bit is shifted to the next more significant position.

The LS181 is an arithmetic logic unit (ALU) function generator that has a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in Tables (a) and (b) at 1.1. These operations are selected by the four function-select lines (S0, S1, S2 and S3) and include addition, subtraction, decrement and straight transfer.

When performing arithmetic manipulations, the internal carries must be enabled by applying a Low level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the '182' full carry look-ahead circuit, high-speed arithmetic operations can be performed.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output ($C_n + 4$) are available. However, the ripple-carry delay has also been minimised so that arithmetic manipulations for small word lengths can be performed without external circuitry. The 'LS181' will accommodate active-High or active-Low data if the pin designations are interpreted at follows:-

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low data (Table A)	$\bar{A}_0$	$\bar{B}_0$	$\bar{A}_1$	$\bar{B}_1$	$\bar{A}_2$	$\bar{B}_2$	$\bar{A}_3$	$\bar{B}_3$	$\bar{F}_0$	$\bar{F}_1$	$\bar{F}_2$	$\bar{F}_3$	C_n	C_n+4	$\bar{P}$	$\bar{G}$
Active-High data (Table B)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\bar{C}_n$	$\bar{C}_n+4$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is $A-B-1$, which requires an end-around or forced carry to provide $A-B$.

The 'LS181' can also be utilised as a comparator. The $A = B$ output is internally decoded from the function outputs (F_0, F_1, F_2, F_3) so that when two words of equal magnitude are applied at the A and B outputs, it will assume a High level to indicate equality ($A = B$). The ALU should be in the subtract mode with $C_n = H$ when performing the comparison. The $A = B$ output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ($C_n + 4$) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S_3, S_2, S_1, S_0 at L, H, L, L, respectively.

INPUT C_n	OUTPUT C_n+4	ACTIVE-LOW DATA (Figure 1)	ACTIVE-HIGH DATA (Figure 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

This circuit has been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four-function-select inputs (S_0, S_1, S_2, S_3) with the mode control input (M) at a High level to disable the internal carry. The 16 logic functions are detailed in Tables (A) and (B) and include exclusive-OR, NAND, AND, NOR and OR functions.

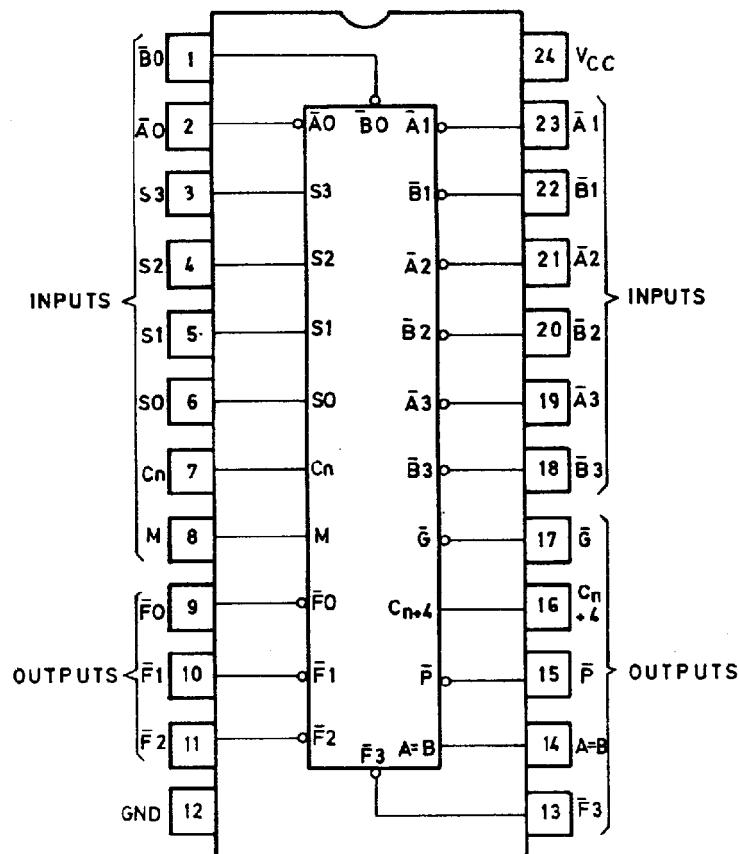
Signal Designations

The 'LS181' together with the '182' can be used with the signal designations of either diagram (a) or (b) in Appendix A1.3. The inversion indicators (0) and the bars over the terminal letter symbols (e.g. C) each indicate that the associated input or output is active with respect to the selected function of the device when that input or output is Low. That is, a Low at $\bar{C}$ means 'do carry' while a High means 'do not carry'.

The logic functions and arithmetic operation obtained with signal designations of diagram (a) Appendix A1.3 are given in Table (A). Those obtained with signal designations of diagram (b) Appendix A1.3 are given in Table (B).

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Arithmetic logic units/function generators

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS181J	N	W
-25 + 85	84LS181J		
-40 + 85	64LS181J		
-55 +125	54LS181J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V	(
2.2	Maximum input voltages								
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V	
2.2.2	Maximum input voltage between multiple emitter transistor input	V_{II}						+5,5V	
					54LS	64LS	74LS	84LS	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85		
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)				

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum value of High level input voltage	V_{IHA}	54LS 64/74/84LS	5,5 5,25	V V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of High level output current A = B output only	I_{OHX}	All types	100,0	μ A
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μ A
Maximum value of off-level voltage	V_{OZA}	All types	5,5	V
D.C. noise margin				
at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	All types	0,7	V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T_{amb} min.	-55	-40	0	-25	$^{\circ}\text{C}$
T_{amb} max.	+125	+85	+70	+85	
V_{CC} min.	4,5	4,75			V
V_{CC} max.	5,5	5,25			

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	Condition A: All outputs open circuit S0 through S3, M and A inputs at 4,5V. Other inputs grounded.					
	54LS	$V_{CC} \text{ max.}$	I_{CC}	-	32,0	mA
	64/74/84LS	$V_{CC} \text{ max.}$	I_{CC}	-	34,0	mA
	Condition B: S0 through S3 and M are at 4,5V. All other inputs grounded.					
	54LS	$V_{CC} \text{ max.}$	I_{CC}	-	35,0	mA
	64/74/84LS	$V_{CC} \text{ max.}$	I_{CC}	-	37,0	mA
High level input current	$V_{IH(1)} = V_{IHA}$					
	Mode input	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,1	mA
	Any $\bar{A}$ or $\bar{B}$ input	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,3	mA
	Any S input	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,4	mA
	Carry input	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,5	mA
	$V_{IH(2)} = 2,7V$					
	Mode input	$V_{CC} \text{ max.}$	$I_{IH(2)}$	-	20,0	μA
	Any $\bar{A}$ or $\bar{B}$ input	$V_{CC} \text{ max.}$	$I_{IH(2)}$	-	60,0	μA
Low level input current	$V_{IL} = 0,4V$ to each input in turn, other related inputs at $V_{IH} \text{ max. value.}$					
	Mode input	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
	Any A or B input	$V_{CC} \text{ max.}$	$-I_{IL}$	-	1,2	mA
	Any S input	$V_{CC} \text{ max.}$	$-I_{IL}$	-	1,6	mA
Input clamping voltage	Carry input	$V_{CC} \text{ max.}$	$-I_{IL}$	-	2,0	mA
	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V