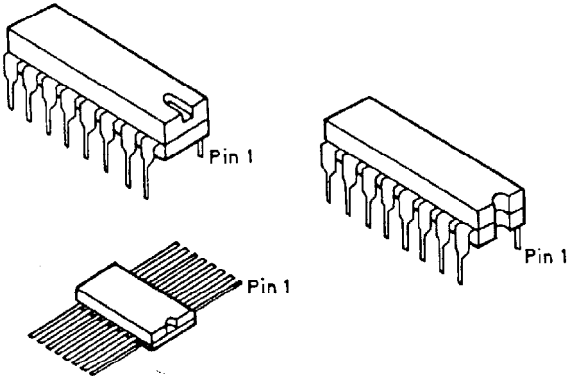


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	BS CECC 90103 - 080 ISSUE 1 NOVEMBER 1981  Page 1 of 21 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS190 64LS190 74LS190 84LS190
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 SYNCHRONOUS UP/DOWN B.C.D. COUNTER WITH MODE CONTROL TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.1 Truth table (contd)

	INPUTS								OUTPUTS					
	LOAD	CLOCK	ENABLE G	DOWN UP	A	B	C	D	Q _A	Q _B	Q _C	Q _D	RIPPLE CLOCK	MAX. MIN.
LOAD	L	X	X	X	A	B	C	D	Q _A	Q _B	Q _C	Q _D	H	L
	L	X	L	L	H	H	H	L	H	H	H	L	H	L
COUNT UP	H	↑	L	L	X	X	X	X	L	L	L	H	H	L
	H	↑	L	L	X	X	X	X	H	L	L	H	H	H
	H	↓	L	L	X	X	X	X	H	L	L	H	L	H
	H	↑	L	L	X	X	X	X	L	L	L	L	H	L
	H	↑	L	L	X	X	X	X	H	L	L	L	H	L
	H	↑	L	L	X	X	X	X	L	H	L	L	H	L
INHIBIT	H	H	↑	L	X	X	X	X	L	H	L	L	H	L
	H	↑	H	L	X	X	X	X	L	H	L	L	H	L
	H	H	H	↑	X	X	X	X	L	H	L	L	H	L
	H	↑	H	H	X	X	X	X	L	H	L	L	H	L
	H	H	↓	H	X	X	X	X	L	H	L	L	H	L
COUNT DOWN	H	↑	L	H	X	X	X	X	H	L	L	L	H	L
	H	↑	L	H	X	X	X	X	L	L	L	L	H	H
	H	↓	L	H	X	X	X	X	L	L	L	L	L	H
	H	↑	L	H	X	X	X	X	H	L	L	H	H	L
	H	↑	L	H	X	X	X	X	L	L	L	H	H	L
	H	↑	L	H	X	X	X	X	H	H	H	L	H	L

↓ = High to Low transition of clock

↑ = Low to High transition of clock

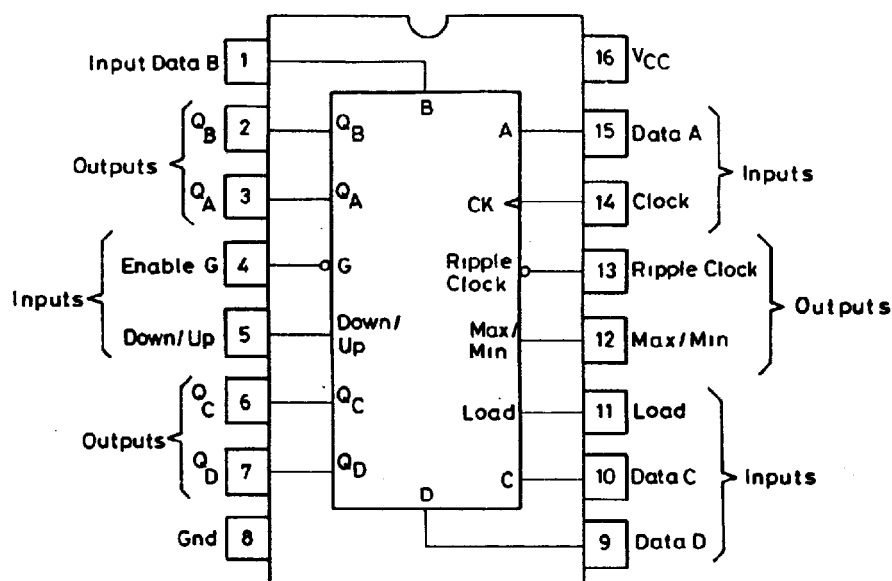
H = High level

L = Low level

X = Logic level irrelevant

1.2 Terminal identification, type designation and marking

1.2.1 Terminal Identification



The counter is a synchronous, 4-bit reversible B C D counter having a Ripple Clock and Max./Min. outputs to perform the cascading function. Synchronous operation is provided by simultaneous clocking of the four J-K bistables so that the outputs (Q_A to Q_D) change coincident with each other when so instructed by the steering logic. Bistable outputs are triggered by a Low to High transition of the Clock input when the Enable input is Low. If the enable input is held High, counting is inhibited. Level changes at the Enable input should be made only when the Clock input is High. The direction of the count is determined by the level of the Down/Up input; when Low, the counter counts up and when High, it counts down.

Counter outputs may be preset by entering the desired data at the Data inputs (A, B, C, D) while the load input is Low. The output will change to agree with the Data inputs independently of the Clock input. The Clock Down/Up and Load inputs are buffered to lower the drive requirement.

The Ripple Clock output produces a Low-level pulse, equal in width to the Low-level portion of the Clock input, when the counter attains minimum or maximum count for cascading, this output can be fed to the Enable input of a succeeding counter if parallel clocking is used, or to the Clock input if parallel enabling is used.

The Max./Min. output produces a High-level pulse, approximately equal in width to one complete cycle of the Clock input, when the counter attains minimum or maximum count. The output can be used to achieve 'Look-ahead' for high speed operation.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS190J	N	W
-25 + 85	84LS190J		
-40 + 85	64LS190J		
-55 +125	54LS190J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type code
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V
2.2	Maximum input voltages		
2.2.1	Maximum input voltage	V_I	-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V

54LS 64LS 74LS 84LS

2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	-55	-40	0	-25
			max.	+125	+85	+70	+85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)		
			max.	+150			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS	4,5 - 5,5	V
		64/74/84LS	4,75 - 5,25	V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS	0,7	V
		64/74/84LS	0,8	V
Maximum value of Low level output current for each output	I_{OLA}	54LS	4,0	mA
		64/74/84LS	8,0	mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL}	All types	0,3	V
	V_{NH}	54LS	0,5	V
		64/74/84LS	0,7	V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IN} = 0V$ (1)	V_{CC} max.	I_{CC}	-	35,0	mA
High level input current						
Enable inputs	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,3	mA
Other inputs				-	0,1	mA
Enable inputs	$V_{IH(2)} = 2,7V$		$I_{IH(2)}$	-	60,0	µA
Other inputs				-	20,0	µA
Low level input current						
Enable inputs	$V_{IL} = 0V$	V_{CC} max.	I_{IL}	-	1,2	mA
Other inputs				-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage						
54LS	$I_{OH} = -400,0\mu A$	V_{CC} min.	V_{OH}	2,5	-	V
64/74/84LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
All types	$I_{OL(1)} = 4,0mA$ (2)		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA$ (3)		$V_{OL(2)}$	-	0,5	V

(1) To all inputs, (2) Fan out = 10, (3) Fan out = 20

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output short circuit current	$V_O = 0V$ (4)	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	ns
Propagation times All types	$T_{amb} = 25^{\circ}C$ test conditions as in Sub-group A5	5,0V				
From Load	To $Q_A Q_B Q_C Q_D$		t_{PHL}	-	50,0	ns
Data A,B,C,D	$Q_A Q_B Q_C Q_D$			-	50,0	ns
Clock	Ripple Clock			-	24,0	ns
Clock	$Q_A Q_B Q_C Q_D$			-	36,0	ns
Clock	Max./Min.			-	52,0	ns
Down/Up	Ripple Clock			-	45,0	ns
Down/Up	Max./Min.			-	33,0	ns
Enable	Ripple Clock			-	33,0	ns
From Load	To $Q_A Q_B Q_C Q_D$		t_{PLH}	-	33,0	ns
Data A,B,C,D	$Q_A Q_B Q_C Q_D$			-	32,0	ns
Clock	Ripple Clock			-	20,0	ns
Clock	$Q_A Q_B Q_C Q_D$			-	24,0	ns
Clock	Max./Min.			-	42,0	ns
Down/Up	Ripple Clock			-	45,0	ns
Down/Up	Max./Min.			-	33,0	ns
Enable	Ripple Clock			-	33,0	ns
Maximum clock frequency			$f_{(clock)}$	20,0	-	MHz
Duration of clock pulse			$t_{p(clock)}$	25,0	-	ns
Duration of load input pulse			$t_{p(load)}$	35,0	-	ns
Data set-up time			t_{set-up}	20,0	-	ns
Data hold time			t_{hold}	5,0	-	ns
Count enable time			t_{enable}	40,0	-	ns

(4) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See 3.2.1 of this specification