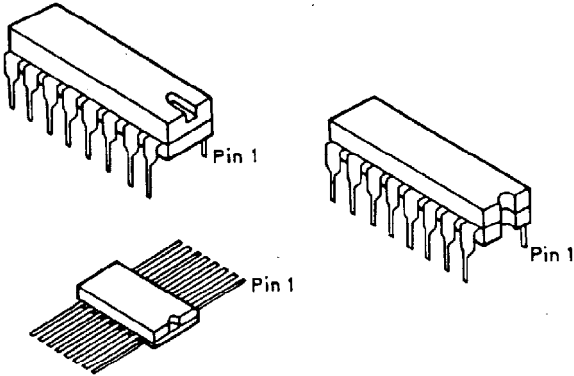


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	BS CECC 90103 - 081 ISSUE 1 NOVEMBER 1981  Page 1 of 19 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS192 64LS192 74LS192 84LS192
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 SYNCHRONOUS 4-BIT UP/DOWN DUAL CLOCK BCD COUNTER TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

Load Sequence

CLEAR	LOAD	DATA INPUTS				OUTPUTS				CARRY	BORROW
		A	B	C	D	Q _A	Q _B	Q _C	Q _D		
$\overline{1}$	H	A	B	C	D	L	L	L	L	H	H
L	$\overline{1}$	A	B	C	D	A	B	C	D	H	H

Count Sequence

CLEAR	LOAD	COUNT APPLIED		OUTPUTS				CARRY	BORROW
		UP	DOWN	Q _A	Q _B	Q _C	Q _D		
$\overline{1}$	H			L	L	L	L	H	H
L	H	1		H	L	L	L	H	H
L	H	2		L	H	L	L	H	H
L	H	3		H	H	L	L	H	H
L	H	4		L	L	H	L	H	H
L	H	5		H	L	H	L	H	H
L	H	6		L	H	H	L	H	H
L	H	7		H	H	H	L	H	H
L	H	8		L	L	L	H	H	H
L	H	9		H	L	L	H	H	H
L	H			L	L	L	L	$\overline{1}$	H
$\overline{1}$	H			H	L	L	L	H	H
L	H		9	L	L	L	L	H	$\overline{1}$
L	H		8	L	L	L	H	H	H
L	H		7	H	H	H	L	H	H

$\overline{1}$ = High level clock pulse applied to the Clear input

$\overline{1}$ = Low level clock pulse applied to the Load input or generated at the Carry Borrow output when the counter overflows/underflows. The overflow/underflow pulse width is the same as the Low level portion of the corresponding Count input pulse.

H = High level

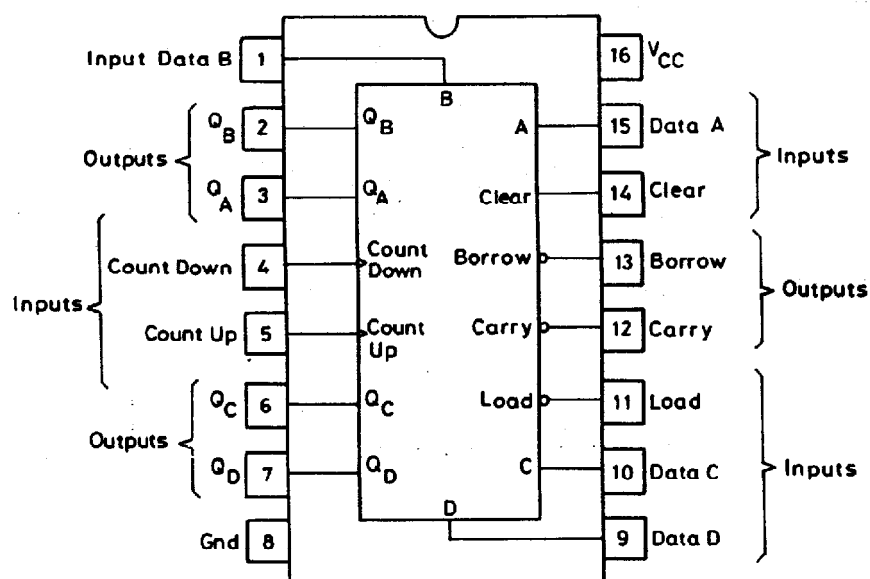
L = Low level

NOTES

- When loading, the outputs are valid after application of the clock pulse.
- For proper clock operation, BCD numbers in excess of 9 should not be loaded.
- Counting occurs on the positive-going edge of the clock pulse.
- The Count inputs are addressed singly, the other Count input being kept High.

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Synchronous 4-bit up/down dual clock BCD counter

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS192J	N	W
-25 + 85	84LS192J		
-40 + 85	64LS192J		
-55 +125	54LS192J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor input	V_{II}						+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	54LS -55 +125	64LS -40 +85	74LS 0 +70	84LS -25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54LS	0,5	V
		64/74/84LS	0,7	V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	V _{CC} (V)	Symbol	Min.	Max.	Unit	
Total supply current per package	All outputs open circuit, clear and load inputs zero volts and other inputs at 4,5V.	V _{CC} max.	I _{CC}	-	34,0	mA	
High level input current	V _{IH} (1) = 7,0V	V _{CC} max.	I _{IH} (1)	-	0,1	mA	
	V _{IH} (2) = 2,7V		I _{IH} (2)	-	20,0	μA	
Low level input current	V _{IL} = 0,4V	V _{CC} max.	-I _{IL}	-	0,4	mA	
Input clamping voltage	-I _{IC} = 18,0mA	V _{CC} = 5,0V	-V _{ICA}	-	1,5	V	
Output voltage		V _{CC} min.					
54LS	I _{OH} = -400,0μA		V _{OH}	2,5	-	V	
64/74/84LS	I _{OH} = -400,0μA		V _{OH}	2,7	-	V	
All types	I _{OL} (1) = 4,0mA (1)		V _{OL} (1)	-	0,4	V	
64/74/84LS	I _{OL} (2) = 8,0mA (2)		V _{OL} (2)	-	0,5	V	
Output short circuit current	V _O = 0V (3)	V _{CC} max.	-I _{OS}	15,0	130,0	mA	
Propagation times	T _{amb} = 25°C* test conditions as in Sub-group A5	5,0V	t _{PLH}				
All types							
From(input) To(output)							
Count-up Carry					-	26,0	ns
Count-down Borrow					-	24,0	ns
Either count Q					-	38,0	ns
Load Q				-	40,0	ns	
From(input) To(output)				t _{PHL}			
Count-up Carry					-	24,0	ns
Count-down Borrow					-	24,0	ns
Either count Q					-	47,0	ns
Load Q					-	40,0	ns
Clear Q					-	35,0	ns
Set-up time				t _{set-up}	20,0	-	ns
Data hold time			t _(hold)	5,0	-	ns	
Duration of clock pulse			t _{p(clock)}	20,0	-	ns	
Maximum clock frequency			f _(clock)	25,0	-	MHz	

(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1$ sec

* See 3.2.1 of this specification