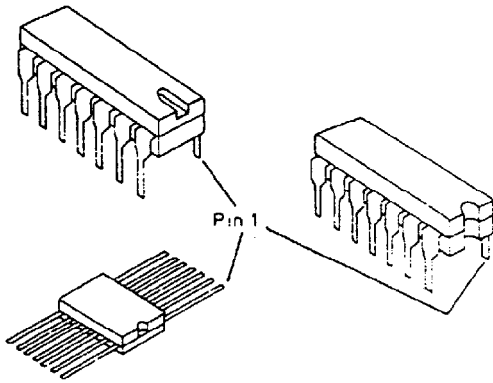


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 085 ISSUE 1 JANUARY 1982  Page 1 of 20 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND 	
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS196 64LS196 74LS196 84LS196 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50B) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	PRESETTABLE DECADE/BI QUINARY COUNTERS/LATCHES TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY
	ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

B.C.D. COUNT SEQUENCE*				
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-QUINARY (5-2)**				
COUNT	OUTPUT			
	Q _A	Q _B	Q _C	Q _D
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = High level

L = Low level

* = Output Q_A is connected to Clock 2 input** = Output Q_B is connected to Clock 1 input

1.1.1 Device description

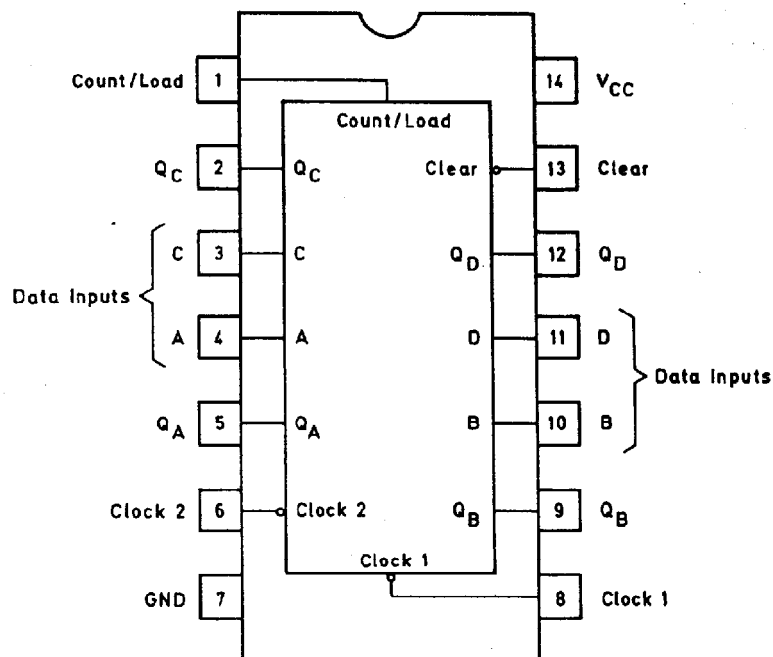
The counters each comprise four master-slave flip-flops which are internally connected to provide a divide-by-two and a divide-by-five counter. The outputs (Q_A, Q_B, Q_C, Q_D) may be preset by taking the Count/Load input low and presenting the required data at the Data inputs (A, B, C, D). The outputs change to agree with the Data inputs independent of the level of either Clock input.

During counting, information is transferred to the outputs on the negative-going edge of the Clock pulse. Application of a Low to the direct Clear input sets all outputs Low regardless of the levels of the Clocks.

The counters can be used as 4-bit latches by using the Count/Load input as the strobe and presenting data at the Data inputs. With the Count/Load Low, the outputs directly follow the Data inputs, but with the Count/Load High and the Clock inputs inactive, the outputs remain unchanged.

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Presettable decade/bi quinary counters/latches

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS196J	N	W
-25 + 85	84LS196J		
-40 + 85	64LS196J		
-55 +125	54LS196J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +0,7V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	54LS -55	64LS -40	74LS 0	84LS -25	
			max.	+125	+85	+70	+85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)			
			max.	+150				

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS	4,5 - 5,5	V
		64/74/84LS	4,75 - 5,25	V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
D.C. noise margin				
at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	All outputs open circuit. Inputs grounded.	V_{CC} max.	I_{CC}	-	27,0	mA
High level input current	$V_{IH(1)} = 5,5V$ Data, Count/Load Clear, Clock 1	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
	Clock 2		$I_{IH(1)}$	-	0,2	mA
			$I_{IH(1)}$	-	0,4	mA
	$V_{IH(2)} = 2,7V$ Data, Count/Load Clear, Clock 1		$I_{IH(2)}$	-	20,0	μA
	Clock		$I_{IH(2)}$	-	40,0	μA
			$I_{IH(2)}$	-	80,0	μA
			$I_{IH(2)}$	-		
Low level input current	$V_{IN} = 0,4V$ to each input in turn, other related inputs at 5,5V Data, Count/Load Clear Clock 1 Clock 2		$-I_{IL}$	-	0,4	mA
			$-I_{IL}$	-	0,8	mA
			$-I_{IL}$	-	2,4	mA
			$-I_{IL}$	-	2,8	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage	54LS $I_{OH} = -400,0\mu A$	V_{CC} min.	V_{OH}	2,5	-	V
	64/74/84LS $I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
	All types $I_{OL(1)} = 4,0mA$ (1)		$V_{OL(1)}$	-	0,4	V
	64/74/84LS $I_{OL(2)} = 8,0mA$ (2)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ (3) $V_{IN} = 0V$ or 4,5V**	V_{CC} max.	$-I_{OS}$	15,0	130,0	mA
Propagation times	$T_{amb} = 25^{\circ}C$ *	5,0V				
All types	test conditions as in Sub-group A5					
High to Low level	Clock 1 to Q_A		t_{PHL}	-	20,0	ns
	Clock 2 to Q_B		t_{PHL}	-	33,0	ns
	Clock 2 to Q_C		t_{PHL}	-	62,0	ns
	Clock 2 to Q_D		t_{PHL}	-	45,0	ns

(1) Fan out = 10, (2) Fan out = 20,
(3) Only one output at a time, duration $t \leq 1$ sec

*See 3.2.1 of this specification

**Refer to truth table

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
High to Low level (contd)	A/B/C/D to $Q_A, Q_B,$ Q_C, Q_D		t_{PHL}	-	44,0	ns
	Load to Any output		t_{PHL}	-	45,0	ns
	Clear to Any output		t_{PHL}	-	51,0	ns
Low to High level	Clock 1 to Q_A		t_{PLH}	-	15,0	ns
	Clock 2 to Q_B		t_{PLH}	-	24,0	ns
	Clock 2 to Q_C		t_{PLH}	-	57,0	ns
	Clock 2 to Q_D		t_{PLH}	-	30,0	ns
	A/B/C/D to $Q_A, Q_B,$ Q_C, Q_D		t_{PLH}	-	30,0	ns
	Load to Any output		t_{PLH}	-	41,0	ns
Maximum clock frequency	Clock to Q_A		$f_{(clock)}$	30,0	-	MHz
Maximum duration of input pulse	Clock 1		t_p	20,0	-	ns
	Clock 2		t_p	30,0	-	ns
	Clear		t_p	15,0	-	ns
	Load		t_p	20,0	-	ns
Set-up times (input hold times) WRT $\uparrow$ positive edge of load pulse	High level data		t_{set-up}	10,0	-	ns
	Low level data		t_{set-up}	15,0	-	ns
Hold times WRT $\uparrow$ positive edge of load pulse	High level data		t_{hold}	0	-	ns
	Low level data		t_{hold}	6,0	-	ns
Count enable time	Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the Count/ Load and clear inputs must both be High to ensure counting		t_{enable}	30,0	-	ns