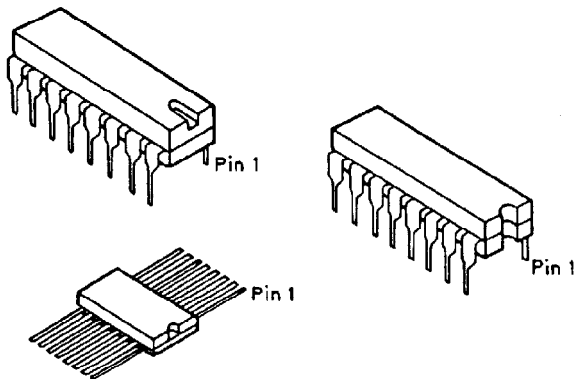


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 086 ISSUE 1 NOVEMBER 1981
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	 Page 1 of 22 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS221 64LS221 74LS221 84LS221
Outline not to scale: Isometric projection Marking information see clause 1 	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT TRIGGER INPUTS
	TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY
	ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⌊	⌋
H	↓	H	⌊	⌋
↑	L	H	⌊	⌋

H = High level

L = Low level

X = Logic level irrelevant

↓ = Transition from High to Low level

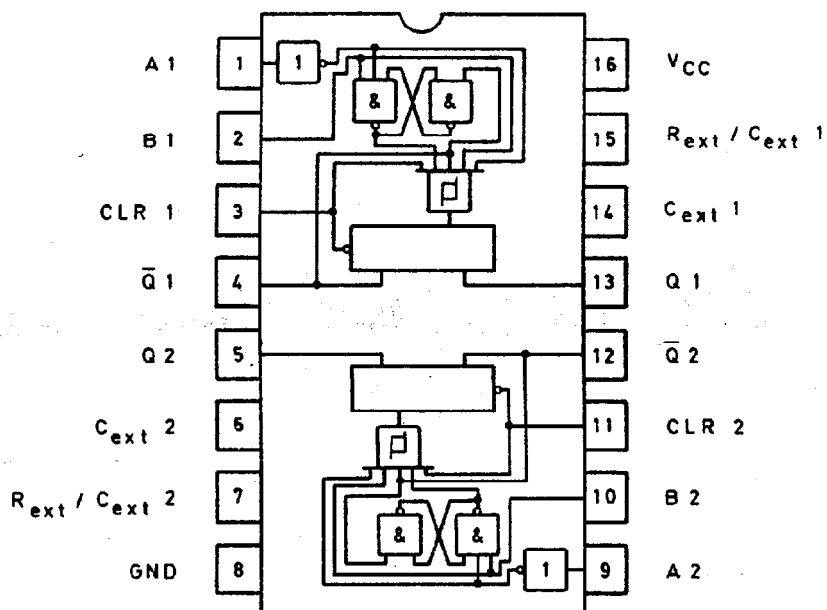
↑ = Transition from Low to High level

⌊ = One high level pulse

⌋ = One low level pulse

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Dual monostable multivibrators
with schmitt trigger inputs

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS221J	N	W
-25 + 85	84LS221J		
-40 + 85	64LS221J		
-55 +125	54LS221J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
				54LS	64LS	74LS	84LS	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85	0 +70	-25 +85		
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)				

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

3.1 (contd)

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum input voltage levels	V_{IN}	All types	-0,3	V
Maximum input voltage levels	V_{INA}	All types	7,0	V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V

3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IN} = 0V$ (1)	$V_{CC} \text{ max.}$				
Quiescent			I_{CC}	-	11,0	mA
Triggered			I_{CC}	-	27,0	mA
High level input current	$V_{IN} = 7,0V$ Other inputs at 0V Outputs open circuit	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,1	mA
	$V_{IN} = 2,7V$	$V_{CC} \text{ max.}$	$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IN} = 0,4V$ Other inputs at V_{IHA} Outputs open circuit	$V_{CC} \text{ max.}$				
Input A			$-I_{ILA}$	-	0,4	mA
Input B			$-I_{ILA}$	-	0,8	mA
Clear			$-I_{ILA}$	-	0,8	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage						
54LS	$-I_{OH} = 400,0\mu A$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
64/74/84LS	$-I_{OH} = 400,0\mu A$		V_{OH}	2,7	-	V
All types	$I_{OL(1)} = 4,0mA$ (2)	$V_{CC} \text{ min.}$	$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA$ (3)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_{IN} = 0V$ or 4,5V as appropriate $V_O = 0V$ (4)	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Positive-going threshold voltage Input A and B			V_{T+}	-	2,0	V

(1) To all inputs, (2) Fan out = 10, (3) Fan out = 20,

(4) Only one output at a time, duration $t \leq 1 \text{ sec}$

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Negative-going threshold voltage Input A and B 54LS 64/74/84LS			V_{T-}	0,7 0,8	- -	V V
Propagation times All types A to $\overline{Q}$ B to $\overline{Q}$ Clear to Q A to Q B to Q Clear to $\overline{Q}$	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5 $C_{ext} = 80pF$ $R_{ext} = 2k\Omega$	5,0V	t_{PHL} t_{PLH} 	- - - - - -	80,0 65,0 55,0 70,0 55,0 65,0	ns ns ns ns ns ns
Maximum pulse width A to Q and $\overline{Q}$ B to Q and $\overline{Q}$ A to Q and $\overline{Q}$ B to Q and $\overline{Q}$ A to Q and $\overline{Q}$ B to Q and $\overline{Q}$ A to Q and $\overline{Q}$ B to Q and $\overline{Q}$	$C_{ext} = 80pF$ $R_{ext} = 2k\Omega$ $C_{ext} = 0$ $R_{ext} = 2k\Omega$ $C_{ext} = 100pF$ $R_{ext} = 10k\Omega$ $C_{ext} = 1\mu F$ $R_{ext} = 10k\Omega$		$t_{p(out)}$ $t_{p(out)}$	70,0 20,0 600,0 6,0	150,0 70,0 750,0 7,5	ns ns ns ns
Maximum input pulse width Clear A and B			$t_{p(in)}$	40,0	-	ns
Clear-inactive-level set-up time			$t_{(set-up)}$	15,0	-	ns
External timing resistor 54LS 64/74/84LS			R_{ext} R_{ext}	1,4 1,4	70,0 100,0	k Ω k Ω
External timing capacitor			C_{ext}	0	1000,0	pF

*See 3.2.1 of this specification