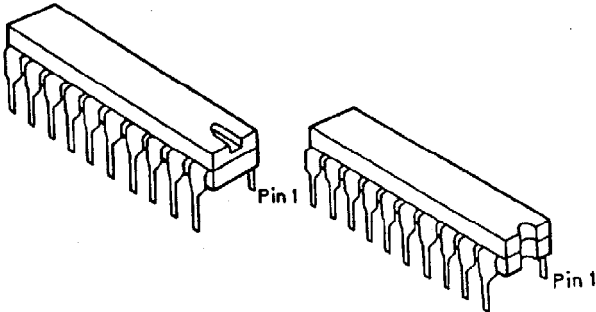


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 087 ISSUE 1 JANUARY 1982 Page 1 of 19 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	 MANUFACTURERS TYPE NUMBER 54LS240 64LS240 74LS240 84LS240
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977 Outline not to scale: Isometric projection Marking information see clause 1  refer to Appendix A1.3 Dual-in-Line (ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 OCTAL BUFFERS/LINE DRIVERS WITH INVERTED 3-LEVEL OUTPUTS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table

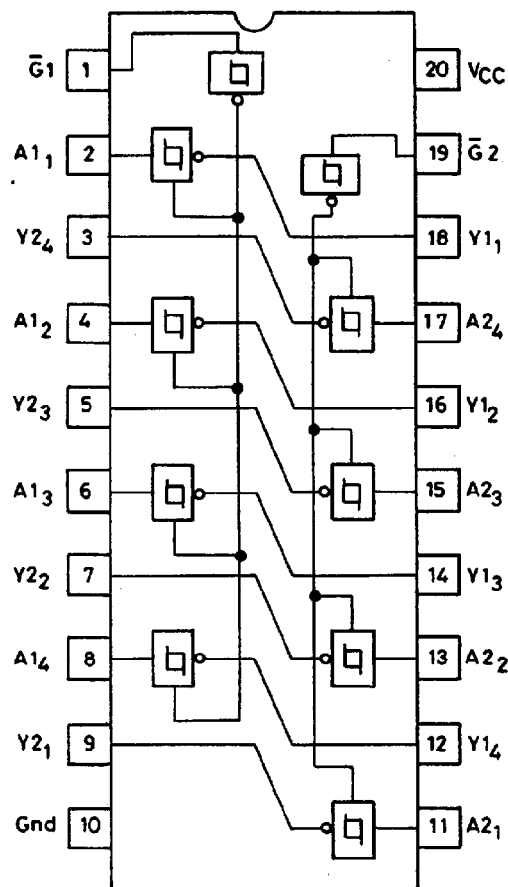
INPUTS		OUTPUT
ENABLE $\bar{G}$	A	Y
H	X	Z
L	L	H
L	H	L

H = High level
 L = Low level
 Z = High-impedance level
 X = Logic level irrelevant

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Octal buffers/line drivers/inverted with 3-level outputs

Three level device

A device whose output can be driven into a High, Low or high-impedance level.

High-impedance level

That level of a device in which the output acquires a high-impedance characteristic.

High-impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high-impedance level.

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS240J	N	W
-25 + 85	84LS240J		
-40 + 85	64LS240J		
-55 +125	54LS240J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}					-0,5V +7,0V
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I					-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}					+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	54LS -55 +125	64LS -40 +85	74LS 0 +70	84LS -25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	12,0 24,0	mA mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	54LS 64/74/84LS	12,0 15,0	mA mA
High impedance level output (leakage) current at 2,7V at 0,4V	I_{OHZ} $-I_{OLZ}$	All types All types	20,0 20,0	μA μA
Maximum applied off-level voltage	V_{OZA}	All types	5,5	V
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V
Hysteresis (at $V_{T+} - V_{T-}$)	V_{HSTB}	All types	0,2	V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	Outputs High	V_{CC} max.	I_{CCH}	-	27,0	mA
	Outputs Low		I_{CCL}	-	44,0	mA
	Outputs Disabled		I_{CCZ}	-	50,0	mA
High level input current	$V_{IH(1)} = 7,0V$ Output control = V_{ILA}	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
	$V_{IH(2)} = 2,7V$ Output control = V_{ILA}		$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4V$ to each input in turn, other related inputs at 4,5V	V_{CC} max.	$-I_{IL}$	-	0,20	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output voltage		V_{CC} min.				
54LS	$I_{OH} = -3,0mA$		V_{OH}	2,4	-	V
64/74/84LS	$I_{OH} = -I_{OHA}$		V_{OH}	2,0	-	V
All types	$I_{OL(1)} = 12,0mA$ (1)		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 24,0mA$ (2)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_{IN} = 0V$ or 4,5V as appropriate** $V_O = 0V$ (3)	V_{CC} max.	$-I_{OS}$	40,0	225,0	mA
Propagation times	$T_{amb} = 25^{\circ}C$ test conditions as in Sub-group A5	5,0V				
All types			t_{PHL}	-	18,0	ns
			t_{PLH}	-	14,0	ns
High-impedance to Low level (Output enable)			t_{PZL}	-	30,0	ns
High-impedance to High level (Output enable)			t_{PZH}	-	23,0	ns
Low level to high-impedance (Output disable)			t_{PLZ}	-	25,0	ns
High level to high-impedance (Output disable)			t_{PHZ}	-	18,0	ns

(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1$ sec

*See 3.2.1 of this specification

**Refer to truth table

3.3 Supplementary information