

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

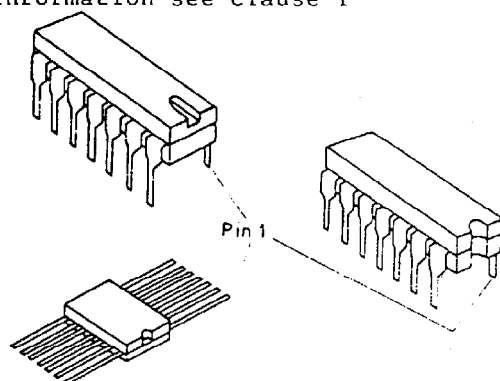
BS CECC 90103 - 090

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ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:BS CECC 90 000 : 1976
BS CECC 90 100 : 1977Outline not to scale: Isometric projection
Marking information see clause 1Refer to IEC 191-1-50a (type A50B)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)

MANUFACTURERS TYPE NUMBER

54LS243
64LS243
74LS243
84LS243SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1QUADRUPLE BUS TRANSCEIVER
NON-INVERTED WITH 3-LEVEL
OUTPUTSTYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR TTL-LOW-POWER
SCHOTTKYASSESSMENT LEVELS
R, S, T AND V1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

CONTROL INPUTS		DATA PORT STATUS	
$\overline{\text{GAB}}$	GBA	A	B
H	H	O	I
L	H	*	*
H	L	ISOLATED	
L	L	I	O

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

H = High level

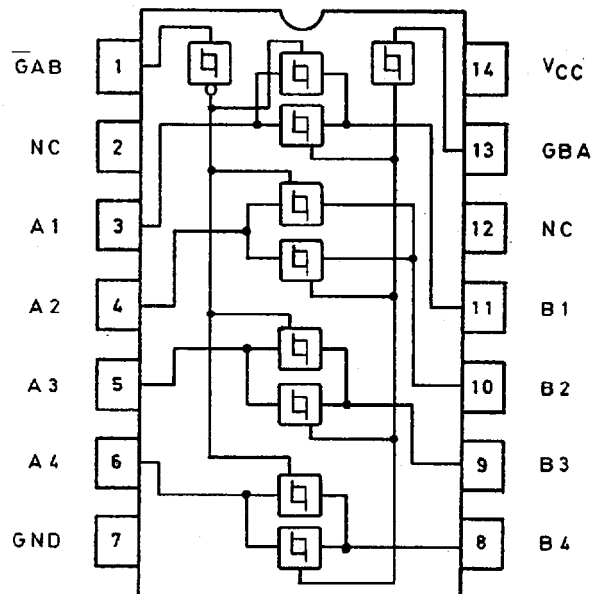
L = Low level

I = Input

O = Output

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



NC = Not Connected

Quadruple bus transceivers non-inverted 3-level outputs

Terminals marked with NC are not connected internally and may be used as electrical support points. The applied voltage shall not exceed 7,0V.

Three level device

A device whose output can be driven into a High, Low or High-impedance level.

High-impedance level

That level of a device in which the output acquires a high-impedance characteristic.

High-impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high-impedance level.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS243J	N	W
-25 + 85	84LS243J		
-40 + 85	64LS243J		
-55 +125	54LS243J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}					-0,5V +7,0V
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I				GA or GB A or B	-0,5V +7,0V +5,5V +5,5V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}					
				54LS	64LS	74LS	84LS
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	12,0 24,0	mA mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	54LS 64/74/84LS	12,0 15,0	mA mA
High impedance level output current	I_{OHZ} $-I_{OLZ}$	All types All types	40,0 200,0	μA μA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V
Hysteresis (at $V_{T+} - V_{T-}$)	V_{HSTB}	All types	0,2	V

3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

3.2.1 (contd)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	Outputs High	V_{CC} max.	I_{CCH}	-	38,0	mA
	Outputs Low		I_{CCL}	-	50,0	mA
	Outputs disabled		I_{CCZ}	-	54,0	mA
High level input current	Output control 0V or 4,5V as appropriate to enable outputs. $V_{IH(1)} = 7,0V$ to G or $\bar{G}$ and 5,5V to A or B $V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
			$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4V^*$ to each input in turn, other related inputs at 4,5V A inputs: $\bar{G}AB$ and GBA at 0V* B inputs: GAB and GBA at 4,5V $\bar{G}AB$, GBA inputs: $V_{IN} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,2	mA
			$-I_{IL}$	-	0,2	mA
			$-I_{IL}$	-	0,2	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{IC}$	-	1,5	V

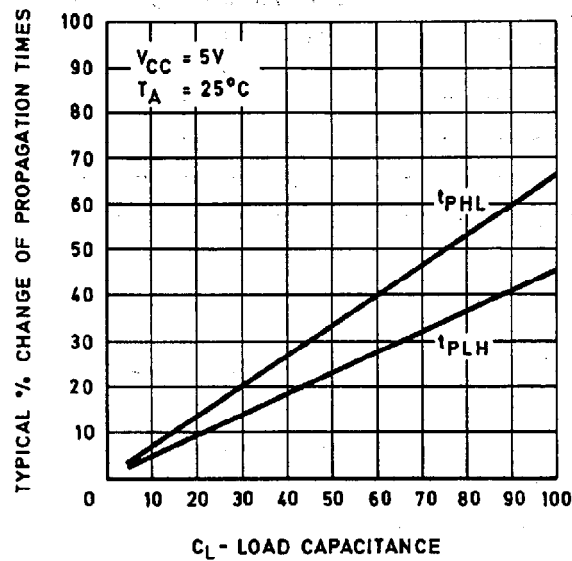
3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output voltage All types 64/74/84LS	$-I_{OH} = 3,0mA$	$V_{CC} \text{ min.}$	V_{OH}	2,4	-	V
	$-I_{OH} = I_{OHA}$		V_{OH}	2,0	-	V
	$I_{OL} = 12,0mA$ (1)		V_{OL}	-	0,4	V
	$I_{OL} = 24,0mA$ (2)		V_{OL}	-	0,5	V
Output short circuit current	$V_{IN} = 0V \text{ or } 4,5V$ $V_O = 0V$ (3)	$V_{CC} \text{ max.}$	$-I_{OS}$	40,0	225,0	mA
Propagation times All types	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
High to Low level			t_{PHL}	-	18,0	ns
Low to High level			t_{PLH}	-	18,0	ns
High impedance to Low level (Output enable)			t_{PZL}	-	30,0	ns
High impedance to High level (Output enable)			t_{PZH}	-	23,0	ns
Low level to High impedance (Output disable)			t_{PLZ}	-	25,0	ns
High level to high impedance			t_{PHZ}	-	18,0	ns

- (1) Fan out = 10, (2) Fan out = 20,
 (3) Only one output at a time, duration $t \leq 1 \text{ sec}$
 *See 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance

3.3.2 Variation of propagation time with temperature

