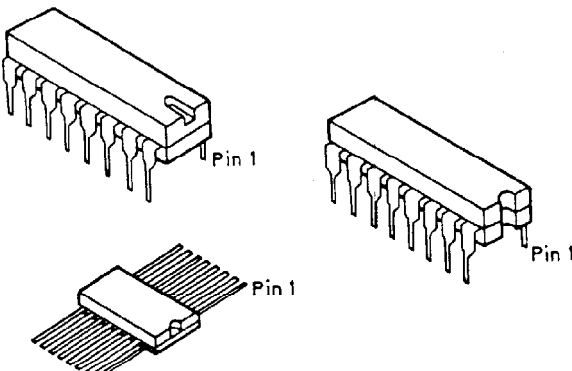


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 096 ISSUE 1 NOVEMBER 1981 Page 1 of 21 pages	
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND		
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS251 64LS251 74LS251 84LS251 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1	
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)		
	8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXERS WITH THREE LEVEL OUTPUTS	
	TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY	
	ASSESSMENT LEVELS R, S, T AND V	

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High level

L = Low level

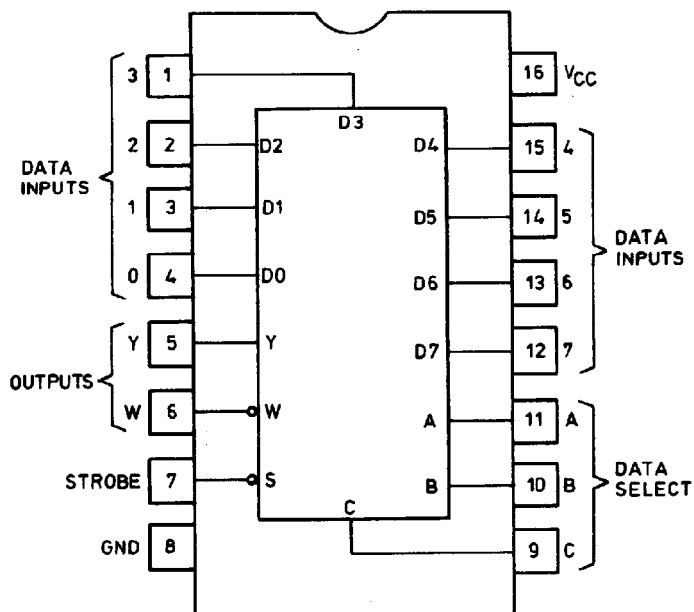
X = Logic level irrelevant

Z = High impedance level (output disabled).

D0, D1.....D7 = The level of the respective D input.

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



8-line to 1-line data selector/multiplexers with three level outputs

Three level device

A device whose output can be driven into a High, Low or high impedance level.

High impedance level

That level of a device in which the output acquires a high impedance characteristic.

High impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high impedance level.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS251J	N	W
-25 + 85	84LS251J		
-40 + 85	64LS251J		
-55 +125	54LS251J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

- | | | | |
|-------|-----------------------------------|----------|----------------|
| 2.1 | Maximum continuous supply voltage | V_{CC} | -0,5V
+7,0V |
| 2.2 | Maximum input voltages | | |
| 2.2.1 | Maximum input voltage | V_I | -0,5V
+7,0V |

2. Limiting conditions of use (contd)

2.2.2 Maximum input voltage between multiple emitter transistor inputs V_{II} +5,5V

			54LS	64LS	74LS	84LS
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85	0 +70	-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	54LS 64/74/84LS	-1,0 -2,6	mA mA
High impedance level output (leakage) current $V_{OUT} = 2,7V$	I_{OHZ}	All types	20,0	μA
High impedance level output (leakage) current $V_{OUT} = 0,4V$	$-I_{OLZ}$	All types	20,0	μA
Maximum value of OFF-level voltage	V_{OZA}	All types	5,5	V
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) AT High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(\text{V})$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IN} = 4,5\text{V}$ to strobe input.	V_{CC} max.	I_{CC}	-	12,0	mA
	$V_{IN} = \text{zero volts}$ to strobe input. All other inputs at 4,5V		I_{CC}	-	10,0	mA
High level input current	$V_{IH(1)} = 7,0\text{V}$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
	$V_{IH(2)} = 2,7\text{V}$	V_{CC} max.	$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4\text{V}$ to each input in turn other inputs at 4,5V	V_{CC} max.	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0\text{mA}$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage All types 64/74/84LS	$I_{OH} = -I_{OHA}$	V_{CC} min.	V_{OH}	2,4	-	V
	$I_{OL(1)} = 4,0\text{mA}^{(1)}$		$V_{OL(1)}$	-	0,4	V
	$I_{OL(2)} = 8,0\text{mA}^{(2)}$		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0\text{V}^{(3)}$	V_{CC} max.	$-I_{OS}$	15,0	130,0	mA

(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1$ sec

3.2.2 (contd)

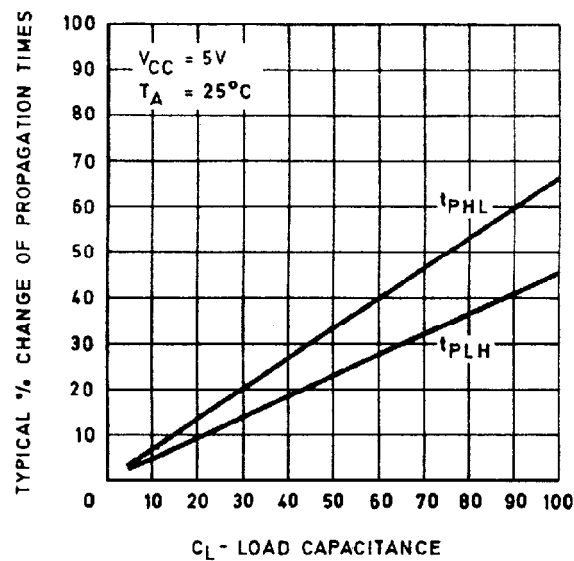
Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
High impedance level output (leakage) current	$V_{IN} = 2,0V$ to strobe input. Other inputs at V_{IHB} or V_{ILA} as appropriate $V_O = 0,4$ or $2,7V^{**}$	V_{CC} max.	$-I_{OLZ}$	-	20,0	μA
			I_{OHZ}	-	20,0	μA
Propagation times All types	$T_{amb} = 25^{\circ}C^{*}$ test conditions as in Sub-group A5	5,0V				
Inputs A, B or C to Y (4 levels of delay)			t_{PLH}	-	45,0	ns
Inputs A, B or C to W (3 levels of delay)			t_{PLH}	-	33,0	ns
Any data input to Y			t_{PLH}	-	28,0	ns
Any data input to W			t_{PLH}	-	15,0	ns
Inputs A, B or C to Y (4 levels of delay)			t_{PHL}	-	45,0	ns
Inputs A, B or C to W (3 levels of delay)			t_{PHL}	-	33,0	ns
Any data input to Y			t_{PHL}	-	28,0	ns
Any data input to W			t_{PHL}	-	15,0	ns
Output enable to High level	Strobe to Y Strobe to W		t_{PZH}	-	45,0	ns
			t_{PZH}	-	27,0	ns
Output enable to Low level	Strobe to Y Strobe to W		t_{PZL}	-	40,0	ns
			t_{PZL}	-	40,0	ns
Output disable from High level ($C_L = 5pF$)	Strobe to Y Strobe to W		t_{PHZ}	-	45,0	ns
			t_{PHZ}	-	55,0	ns
Output disable from Low level ($C_L = 5pF$)	Strobe to Y Strobe to W		t_{PLZ}	-	25,0	ns
			t_{PLZ}	-	25,0	ns

*See 3.2.1 of this specification

**Refer to truth table

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation time Vs. load capacitance

3.2.2 Variation of propagation time with temperature

