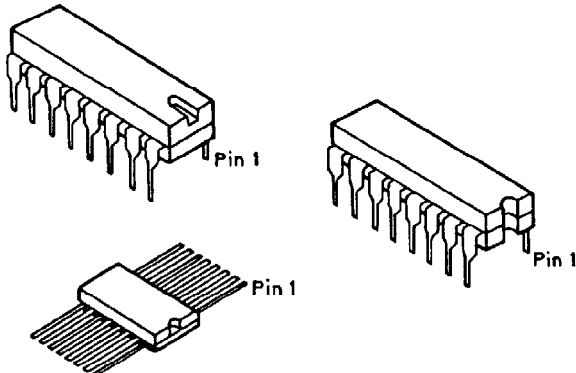


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 099 ISSUE 1 JANUARY 1982  Page 1 of 19 pages	Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977		Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)
	MANUFACTURERS TYPE NUMBER 54LS258A 64LS258A 74LS258A 84LS258A	
	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1	
	QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXERS WITH THREE LEVEL OUTPUTS	
	TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY	
	ASSESSMENT LEVELS R, S, T AND V	

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

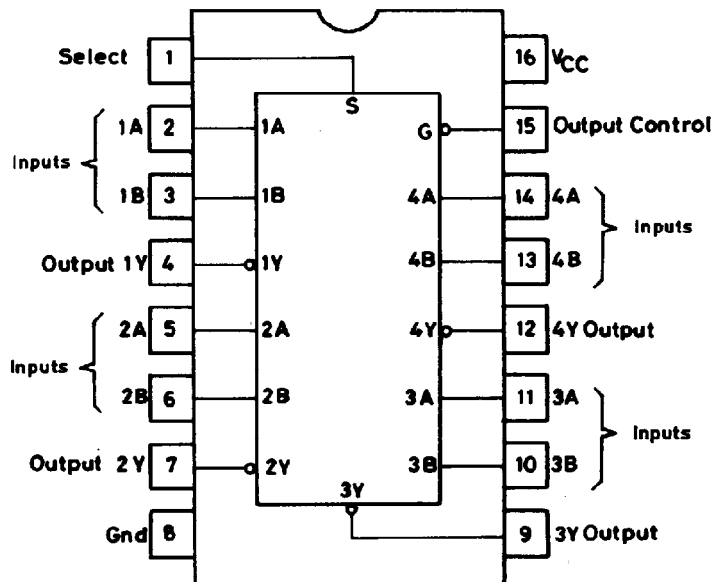
1.1 Truth table (contd)

INPUTS				OUTPUT
OUTPUT CONTROL	SELECT	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level
 L = Low level
 X = Logic level irrelevant
 Z = High impedance level (output disabled)

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Quadruple 2-line to 1-line data selector/
 multiplexers with three level outputs

Three level device

A device whose output can be driven into a High, Low or high-impedance level

High-impedance level

That level of a device in which the output acquires a high-impedance characteristic

High-impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high-impedance level

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS258AJ	N	W
-25 + 85	84LS258AJ		
-40 + 85	64LS258AJ		
-55 +125	54LS258AJ		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1 Maximum continuous supply voltage V_{CC} -0,5V
+7,0V

2.2 Maximum input voltages

2.2.1 Maximum input voltage V_I -0,5V
+7,0V

2.2.2 Maximum input voltage between multiple emitter transistor inputs V_{II} +5,5V

			54LS	64LS	74LS	84LS
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85	0 +70	-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)		

- 3 -

BS CECC 90103 - 099
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3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	12,0 24,0	mA mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	54LS 64/74/84LS	1,0 2,6	mA mA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V V
High impedance level output (leakage)	I_{OHZ} $-I_{OLZ}$	All types All types	20,0 20,0	μA μA
Maximum applied off-level voltage	V_{OZA}	All types	5,5	V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

3.2.1 (contd)

	54LS	64LS	74LS	84LS	
T_{amb} min.	-55	-40	0	-25	°C
T_{amb} max.	+125	+85	+70	+85	
V_{CC} min.	4,5	4,75			V
V_{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(\text{V})$	Symbol	Min.	Max.	Unit
Total supply current per package	I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions	V_{CC} max.				
Outputs Low			I_{CCL}	-	14,0	mA
Outputs High			I_{CCH}	-	7,0	mA
Outputs disabled			I_{CCZ}	-	19,0	mA
High level input current	$V_{IH(1)} = 7,0\text{V}$ S input	V_{CC} max.	$I_{IH(1)}$	-	0,2	mA
	Any input except S		$I_{IH(1)}$	-	0,1	mA
	$V_{IH(2)} = 2,7\text{V}$ S input		$I_{IH(2)}$	-	40,0	μA
	Any input except S		$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4\text{V}$ other inputs at 4,5V S inputs	V_{CC} max.	$-I_{IL}$	-	0,8	V
	Any input except S		$-I_{IL}$	-	0,4	V

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage	$V_{IN} = 2,0V$ or V_{ILA} as appropriate	$V_{CC} \text{ min.}$				
All types	$I_{OH} = -I_{OHA}$		V_{OH}	2,4	-	V
64/74/84LS	$I_{OL(1)} = 12,0mA$ (1)		$V_{OL(1)}$	-	0,4	V
	$I_{OL(2)} = 24,0mA$ (2)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_{IN} = 0V$ $V_O = 0V$ (3)	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
All types						
Low to High level						
From data input to output			t_{PLH}	-	18,0	ns
From select input to output				-	28,0	ns
High to Low level						
From data input to output			t_{PHL}	-	18,0	ns
From select input to output				-	35,0	ns
Output enable to High level			t_{PZH}	-	30,0	ns
Output enable to Low level			t_{PZL}	-	30,0	ns
Output disable from High level	$C_L = 5pF$ $R_L = 667\Omega$		t_{PHZ}	-	30,0	ns
Output disable from Low level	$C_L = 5pF$ $R_L = 667\Omega$		t_{PLZ}	-	25,0	ns

(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1$ sec

*See 3.2.1 of this specification