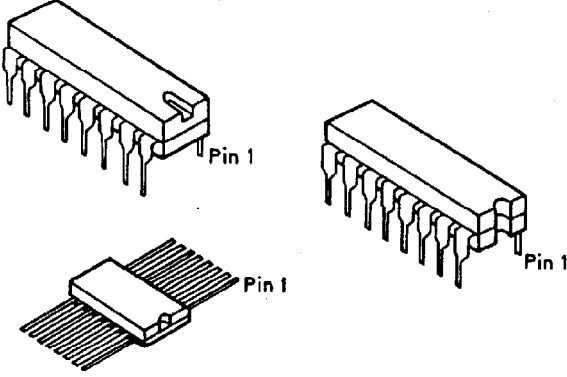


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 100 ISSUE 1 NOVEMBER 1981 Page 1 of 18 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS259 64LS259 74LS259 84LS259 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	8-BIT ADDRESSABLE LATCHES TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200 for details of manufacturers approved to this specification

1.1 Truth table (contd)

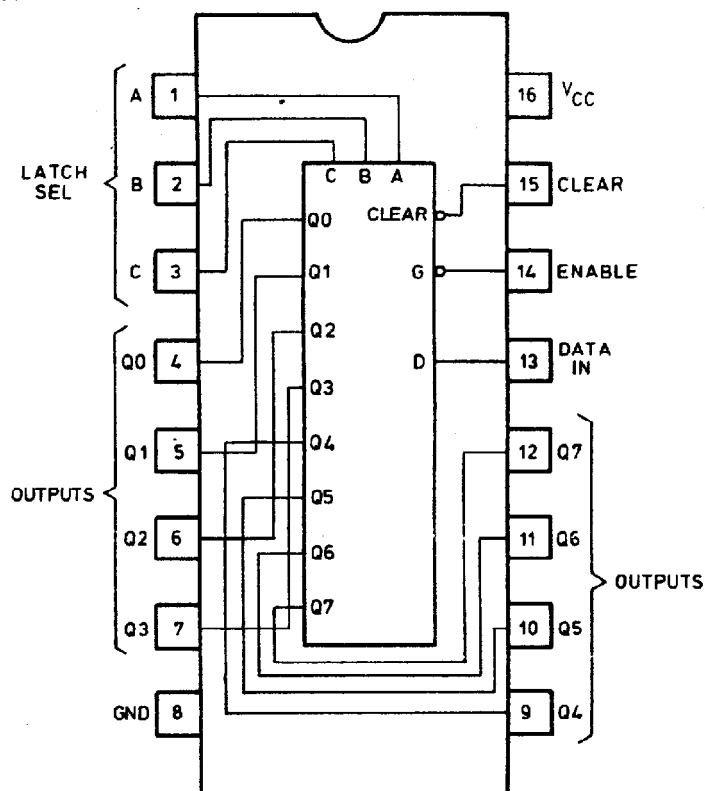
INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	$\bar{G}$			
H	L	D	Q_{i0}	Addressable latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = High level
 L = Low level
 D = The level of the data input
 Q_{i0} = The level of Q_i ($i = 0, 1 \dots 7$, as appropriate before the indicated steady level input conditions were established.)

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



8-bit addressable latches

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS259J	N	W
-25 + 85	84LS259J		
-40 + 85	64LS259J		
-55 +125	54LS259J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	54LS -55 +125	64LS -40 +85	74LS 0 +70	84LS -25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	0,4	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	$I_{OL A}$	54LS 64/74/84LS	4,0 8,0	mA mA

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
DC noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{LHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V

3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	Inputs grounded. Outputs open.	V_{CC} max.	I_{CC}	-	36,0	mA
High level input current	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
	$V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IN} = 0,4V^*$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{IC}$	-	1,5	V

*See 3.2.1 of this specification

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output voltage	$V_{IN} = V_{ILA}^*$ or 2,0V as appropriate**	V_{CC} min.				
54LS	$-I_{OH} = 400,0\mu A$		V_{OH}	2,4	-	V
64/74/84LS	$-I_{OH} = 400,0\mu A$		V_{OH}	2,4	-	V
All types	$I_{OL(1)} = 4,0mA$ (1)		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA$ (2)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_{IN} = 0V^*$ or 4,5V as appropriate** $V_O = 0V$ (3)	V_{CC} max.	$-I_{OS}$	15,0	130,0	mA
Propagation times All types	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
	From To					
	Data Any Q		t_{PHL}	-	21,0	ns
	Address Any Q			-	29,0	ns
	Enable Any Q			-	24,0	ns
	Clear Any Q			-	27,0	ns
	From To					
	Data Any Q		t_{PLH}	-	32,0	ns
	Address Any Q			-	38,0	ns
	Enable Any Q			-	35,0	ns
Pulse width						
Clear			t_P	15,0	-	ns
Enable				15,0	-	ns
Set-up time			t_{set-up}			
Data				15,0†	-	ns
Address				15,0†	-	ns
Hold time			t_{hold}			
Data				5,0†	-	ns
Address				15,0†	-	ns

(1) Fan out - 10, (2) Fan out - 20.

(3) Only one output at a time, duration $t \leq 1$ sec

*See 3.2.1 of this specification

**Refer to truth table

† With reference to the rising edge of the enable pulse